An Improved Modeling and Analysis Technique for Peak Current Mode Control based Boost Converters

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Abstract

A modeling approach is presented that calculates an accurate open loop transfer characteristic for a boost converter that employ peak current-mode control (PCMC). Many techniques exist for modeling a PCMC based boost converter, however all these techniques focus on purely resistive loads and are not always accurate for a purely capacitive load. In this paper a new modeling technique is presented which is simple and gives accurate results for both capacitive and resistive loads. Furthermore, the useful expressions for DC gain and pole locations of a boost converter operating in continuous-conduction mode (CCM) with PCMC are derived and compare well to simulations and measurements.

Index Terms

Boost converter, continuous-conduction mode (CCM), peak current-mode control (PCMC), capacitive load, small-signal transfer function.

List of Symbols

C	Output load capacitance
D	Duty cycle
D'	1-D
F_m	Modulator gain for Ridley's model
$F_h(s)$	Control-to-inductor current transfer function
F_{m1}	Modulator gain for Tan's model
F_{m2}	Modulator gain for Bryant's model
G_0	DC gain
$G_{id}(s)$	Duty-to-inductor current transfer function
$G_{vd}(s)$	Duty-to-output voltage transfer function
$H_e(s)$	Sampling effect in current feedback loop
L	Inductance of the inductor
M_1	Slope of sensed inductor current during on period

M_2	Slope of sensed inductor current during off period
M_c	Slope of external ramp
R_L	Load resistance
R_s	Current sense gain
R_{esr}	Equivalent Series Resistance (ESR) of the capacitor
T_s	Switching period
$T_{co}(s)$	Control-to-output voltage transfer function
V_{dd}	Supply voltage
ω_p	Dominant pole frequency
ω_{rhpz}	Right-Half plane Zero frequency
ω_{zero}	ESR zero frequency
f_s	Switching frequency
i_{Lp}	Peak inductor current
i_L	Inductor current
k_r	Output voltage feedforward gain for Ridley's model
k_{r1}	Output voltage feedforward gain for Tan's model
k_{r2}	Output voltage feedforward gain for Bryant's model
m_c	Slope compensation factor
v_C	Control input voltage
v_O	Output voltage

I. Introduction

PIEZOLECTRIC transducers find countless applications in the area of sound generation, actuation, etc [1]. These transducers can electrically be modeled as capacitive loads and require a high voltage to drive them, which necessitates the use of boost converters in battery powered applications. Maximum efficiency can be achieved by using the boost converter directly to generate the signal for the transducer, avoiding the use of an additional amplifier stage. In order to use a boost converter for signal generation, understanding the dynamics and stability of the system is a crucial step.

Peak current-mode control (PCMC) is a popular control technique for DC-DC converters due to the fast transient response, overload protection, accuracy and ease of compensation. A PCMC based boost converter is shown in Fig 1. With a capacitive load, the output power flow is bidirectional, so the converter can only run in continuous-conduction mode (CCM). The output voltage is sensed via the feedback network of R_{fb1} and R_{fb2} in the compensator to determine the control voltage, where the impedance of the feedback network is much higher than the load impedance. The duty ratio is calculated by comparing the inductor current sensed by the R_s block with the control voltage v_C in the modulator. The duty ratio is then converted to an output voltage by the switching power stage. The PCMC system is a multi-loop system with an inner current loop and an outer voltage loop. The stability of the complete system is highly dependent on the stability of the inner loop, hence

accurately predicting the closed current loop characteristics is very important for stable operation. Many modeling techniques have been developed in the past to effectively predict the small-signal characteristics of switching converters operating with PCMC [2]–[24].

Some of the previous modeling approaches have used exact discrete-time and sampled-data modeling techniques [16]–[23]. However, due to complicated results, they lack insight into simple converter parameters and therefore are difficult to interpret as a circuit designer. Another popular approach is to use continuous time-models [2]–[15]. These modeling techniques use a common methodology in representation of the entire system, but differ mainly in representing the sampling effect and modulator gain. These modeling techniques give very accurate results for classical applications where the load is dominantly resistive and the output capacitor is large to get small ripple. In our case, however, we intend to use the boost converter as a signal generator, necessitating the use of a much smaller output capacitor to increase bandwidth. Furthermore, the piezoelectric load is dominantly capacitive ($R_L = \infty$ in Fig 1). It will be shown that the existing models are less accurate in this case, which motivated us to development a new model. In order to get a highly accurate model of a boost converter for wide load

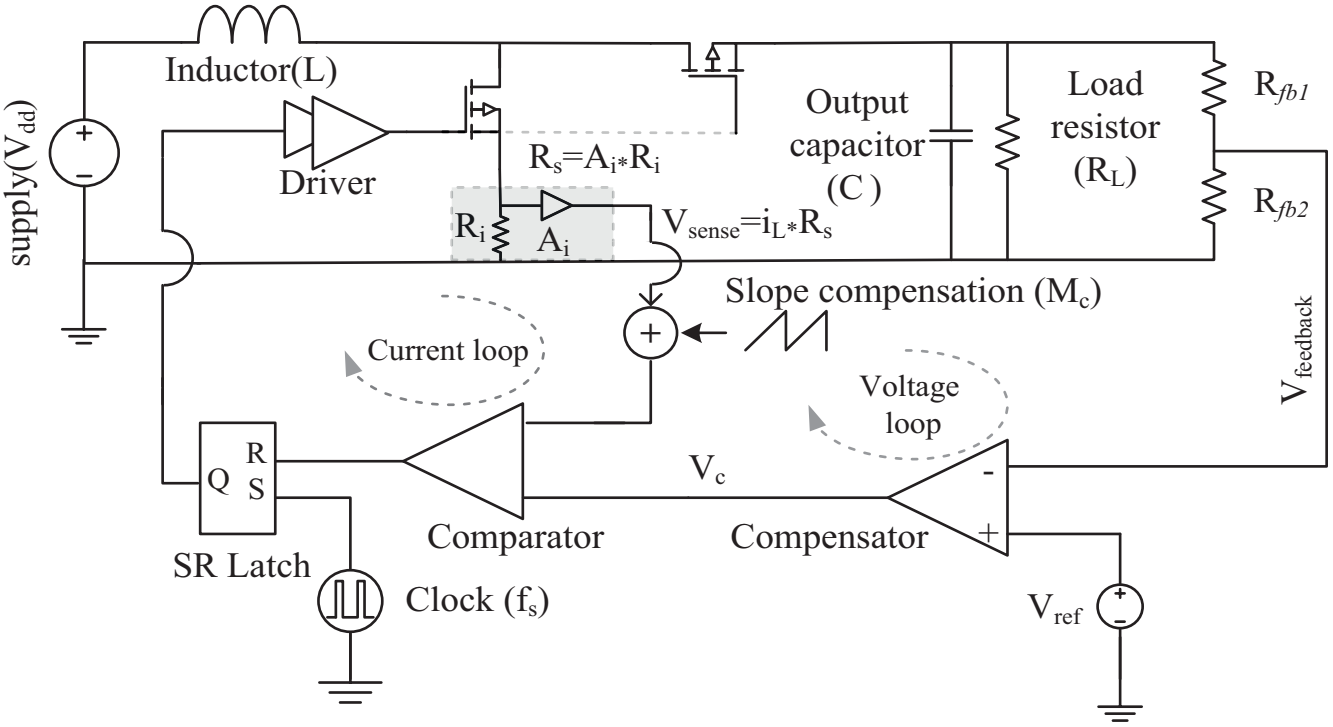


Fig. 1. A peak current-mode control based bi-directional boost converter

variations (for both capacitive and resistive loads), an unambiguous and a simple approach is used here by analyzing the complete converter stage (including closed-current loop) in discrete-time domain and then convert it to continuous-time for better insight into circuit parameters. The new approach doesn't need to separately analyse the current loop and power stage; instead, the closed-current loop is analyzed with capturing the effect of the output voltage simultaneously.

The outline of the paper is as follows: In Section 2, the limitations of existing modeling approaches are discussed in detail. A complete and accurate small-signal model from control-to-output voltage of a PCMC based boost converter with capacitive and resistive load is derived in section 3. Finally, the model is verified and compared with simulation and measurement results.

II. Limitations of Existing Modeling Approaches

To model switched-mode converters, in [2] the complete model is obtained by combining the low-frequency modulator model with a state-space average model of the power stage. This is an interesting technique due to its simplicity but lacks the accuracy to predict the current loop instability at high frequencies. The work proposed in [17] uses sampled-data modeling for the current loop and thus is able to predict the well-known subharmonic oscillations at high frequency. However this technique alone is too complex to be used in practical design. A simplified switch model was proposed in [4] to model the switching power stage and an extension of this model to current-mode control is reported in [24]. This technique achieves good accuracy, but the drawback of using the pulse-width modulation (PWM) switch model and incorporating current-mode control makes the method complex and is generally not straightforward. The injected-absorbed current approach [25] is aimed at providing ease of design and analysis, but provides less accurate results.

A continuous-time model is proposed by Ridley in [7], with the combination of a sampled-data model for the inductor-current loop and a three-terminal switch model for the power stage. This model has been very popular and provides better accuracy than the earlier approaches for both low and high frequencies. The method in [7] lies at the basis of subsequent techniques presented by Tan in [6] and Bryant in [9]. Therefore, this technique is discussed in more detail here.

The circuit in Fig 1 is represented as a block diagram with a closed current-loop [7] and is shown in Fig 2. The power stage is modeled using the duty-to-output voltage transfer $G_{vd}(s)$ and duty-to-inductor current transfer $G_{id}(s)$. The inductor current is sensed and converted to a voltage by the sense block R_s. The sampling effect is represented by $H_e(s)$ and is inserted into the current feedback loop, where (F_m) represents the modulator gain. The effect of the changing output voltage on the current loop is modeled by including an extra feedback path from output to the control voltage defined as output voltage feedforward gain (k_r) [7]. It should be noted that the signals and blocks in this block diagram represent the structure of the model rather than actual physical blocks. In this method, the first step is to calculate basic power stage functions $G_{vd}(s)$ and $G_{id}(s)$. These

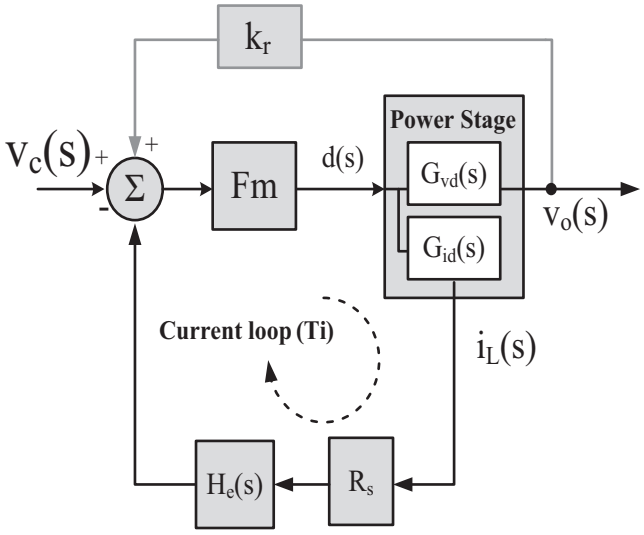


Fig. 2. Block diagram of the modeling approach for PCMC proposed by Ridley [7]

transfer functions can be calculated in different ways, we have used state-space averaging here to calculate the power stage transfer functions for a boost converter stage and the results are formulated as:

$$G_{vd} = \frac{\frac{V_{dd}}{R_L D'^2}({R_L}^2 D'^2 - sR_L L)}{D'^2 R_L + sL + s^2 R_L LC} \tag{1}$$

$$G_{id} = \frac{\frac{V_{dd}}{D'}(2 + sR_L C)}{D'^2 R_L + sL + s^2 R_L LC} \tag{2}$$

In the next step, the control-to-inductor current transfer function is obtained in discrete-time followed by conversion into continuous-time form and is represented as [7]:

$$F_h(s) = \frac{i_l(s)}{v_c(s)} = \frac{1}{R_s}\frac{1+\alpha}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \tag{3}$$

where

$$\alpha = \frac{M_2 - M_c}{M_1 + M_c}$$

Where M_1 is the on time inductor current slope, M_2 is the off time inductor current slope, M_c is the slope of compensation ramp, T_s is the switching period and α defines the slope compensation effect. The same notation will be used for all subsequent derivations.

This model uses $H_e(s)$ to incorporate the high-frequency effects and it is calculated using (3) and is approximated as [7]:

$$H_e(s) \cong 1 + \frac{s}{\omega_n Q} + \frac{s^2}{{\omega_n}^2} \tag{4}$$

where

$$Q = \frac{-2}{\pi} \text{ and } \omega_n = \frac{\pi}{T_s}$$

Ridley [7] presents the modulator gain (Fm) and feedforward gain k_r for the boost converter as:

$$F_m = \frac{1}{(M_1 + M_c)T_s},\ k_r = \frac{D'^2 T_s R_s}{2L} \tag{5}$$

Using the block diagram in Fig 2, the final control-to-output transfer function using Ridley's model can be expressed as:

$$T_{oc}(s) = \frac{F_m G_{vd}(s)}{1 + G_{id}(s)F_m R_s H_e(s) - k_r G_{vd}(s)F_m} \tag{6}$$

The final control-to-output transfer function in (6) can now be calculated using (1), (2), (4) and (5). A similar approach is also presented by Tan in [6], where a different modulator gain (F_{m1}) and the feedforward gain k_{r1} is presented as :

$$F_{m1} = \frac{1}{M_c + \frac{(D'-D)V_{dd}}{2L}(1 + \frac{s}{\omega_p})T_s}, k_{r1} = \frac{DD'T_s}{2L} \tag{7}$$

$$\omega_p = \frac{\omega_n}{Q} \tag{8}$$

$$Q = \frac{1}{\pi(m_c D' - 0.5)} \tag{9}$$

$$m_c = 1 + \frac{M_c}{M_1} \tag{10}$$

The major difference between [7] and [6] is the way the modulator gain, feedforward gain and the high-frequency extension is modeled. The first one uses $H_e(s)$ and the other adds an extra pole in the modulator gain (F_{m1}). Hence Tan's model doesn't consider the sampling effect $H_e(s)$ as a separate block in feedback, but rather combines it within the modulator gain. The third popular approach similar to Tan's model is presented by Bryant in [9], where the modulator gain (F_{m2}) is calculated by using a closed current-loop and the feedforward gain is ignored in this approach. The modulator gain calculated by Bryant includes the sampling effect within the loop and is presented as:

$$F_{m2} = \frac{1}{G_{id}R_s(\frac{sT_s}{1+\alpha}\frac{e^{sT}+\alpha}{e^{sT}-1} - 1)},\ k_{r2} = 0 \tag{11}$$

In order to verify all of the models presented in [6], [7], [9], the models are derived using (6) with their respective modulator gains (F_m, F_{m1}, F_{m2}) and feedforwad gains (k_r, k_{r1}, k_{r2}), and the results are compared in Fig 3 with SIMPLIS simulation. The circuit parameters listed in table I are used with the output capacitance (C) and output resistance (R_L) to represent a typical application using a resistive load. It is interesting to note that the results shown in Fig 3 are indeed very accurate and

TABLE I
CIRCUIT PARAMETERS

Parameters	Values
Duty ratio (D)	0.5
Slope compensation factor (m_c)	1.66
Compensating slope (M_c)	$24mV/\mu$s
On time inductor current sense slope (M_1)	$36mV/\mu$s
Inductor (L)	100 μH
Current sense gain($R_s = R_i \cdot A_i$)	50mΩ*6
Supply voltage (V_{dd})	12V
Switching frequency (f_s)	1MHz
Resistive load ($R_L \| C$)	(50$\Omega \| 10\mu$F)
Capacitive load ($R_L = \infty \| C$)	26nF
Control voltage for capacitive load (Vc)	20mV
Control voltage for resistive load (Vc)	300mV

match well with the simulation results for all the models. To validate the models in [6], [7], [9] for a capacitive load, the output load in the circuit in Fig 1 is replaced by a purely capacitive load ($R_L \longrightarrow \infty$). The static capacitance of the piezo actuator dominates at most frequencies, so a simple capacitor is a fairly accurate representation. Also the value of C is decreased to get sufficient bandwidth (see Table I) and the simulation results are re-evaluated following the same steps as mentioned before. The results are plotted in Fig 4.

The results shown in Fig 4 are not very accurate for low frequencies for Tan's model compared to the simulation, whereas Bryant's model misses the low frequency pole completely. The simulation results for low frequency behaviour predicted by Ridley's model is indeed accurate but shows a 15 degree phase deviation at $f_s/2$ as compared to simulation results. In traditional applications, indeed, the difference at low frequency doesn't drastically affect the overall system design, as they are designed for DC operation only. However, in order to generate dynamically varying signals, like in our case, a more accurate model is important due to the wide variation in duty ratio.

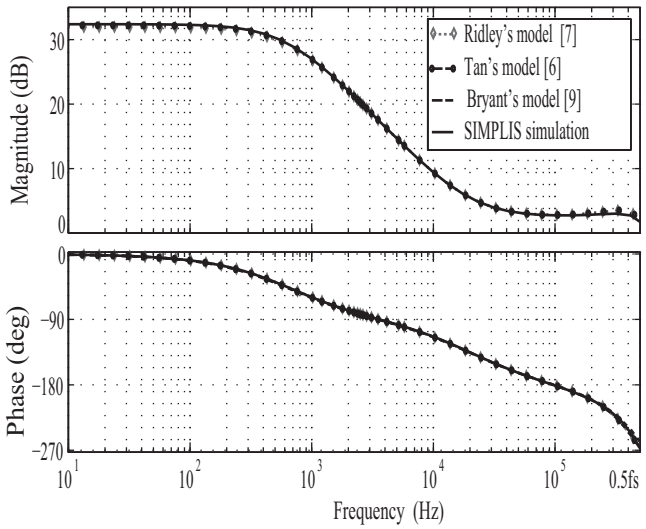


Fig. 3. Comparison of the Ridley [7], Tan [6] and Bryant [9] models control-to-output transfer $T_{co}(s)$ with SIMPLIS simulation for a PCMC boost converter with resistive load ($50\Omega \| 10\mu$F).

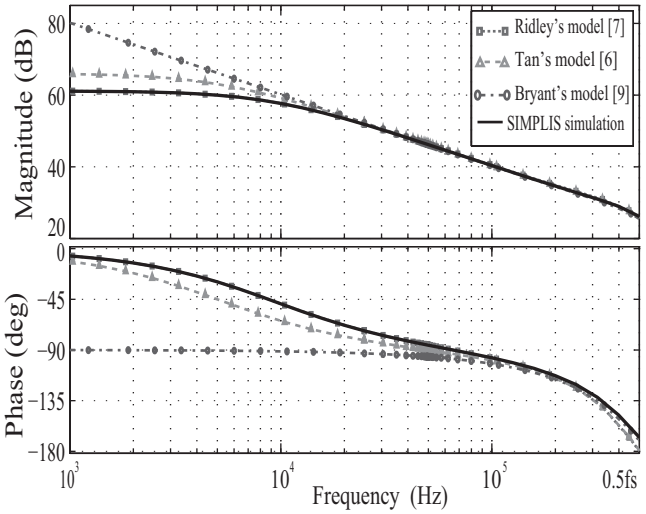


Fig. 4. Comparison of the Ridley [7], Tan [6] and Bryant [9] models control-to-output transfer $T_{co}(s)$ with SIMPLIS simulation for a PCMC boost converter with capacitive load (26nF).

The reason for the deviations between models and simulation can be explained by the choice of different modulator gain F_m, which is a block in a feedback system (Fig 2) of which the behavior depends on the closed loop itself. Therefore it is not as much calculated as selected in [6], [7] allowing for contradictory expressions. In [9], F_m is calculated from the closed loop, but the result is even less accurate as shown above. Therefore it should be noted that the accuracy of these models depends greatly on the way the modulator gain F_m, the gain term k_r and the sampling effect $H_e(s)$ are defined. The inconsistency in these definitions makes the above mentioned methods less attractive. In addition, all of these approaches require the derivation of many blocks, namely F_m, k_r, $G_{vd}(s)$, $G_{id}(s)$ and $H_e(s)$. As an alternative, we present a modeling technique that uses a much more straightforward analysis and provides highly accurate results for both capacitive and resistive loads for both high and low frequencies.

III. Small-Signal Analysis

The complete small-signal model of a PCMC based boost converter consists of the power stage and the closed current-loop. Therefore as a first step, the power stage and the closed current-loop are simultaneously modeled by using a discrete-time approach in subsection A. The resultant discrete-time model is than converted to the continuous-time domain for clear insight into different circuit parameters in subsection B.

A. Discrete-time State Space Modeling

This section derives the control-to-output (T_{co}) transfer function of the PCMC based boost converter for generic load ($R_L \| C$) using discrete-time analysis. The process of determining the transfer function starts with the inspection of the relevant

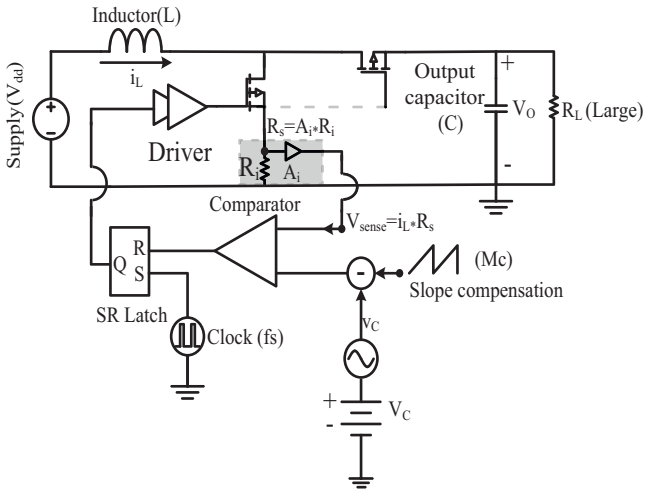


Fig. 5. A closed-current loop PCMC based boost converter with RC ($R_L \| C$) load

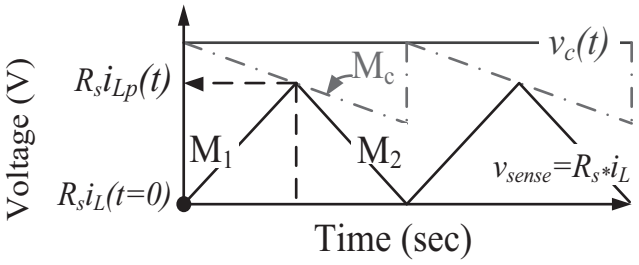
waveforms of the circuit shown in Fig 5. The time-domain waveforms of the PCMC based converter are shown in Fig 6(a), where $R_s i_L$ is a measure for the sensed inductor current and M_1 and M_2 are the sensed inductor current on-time and off-time slopes respectively. In order to dampen the subharmonic oscillations and have a stable operation, a compensating slope M_c is required. Adding slope compensation to the current signal is equivalent to subtracting a slope from the control voltage v_C. The control voltage v_C in combination with the compensating ramp determines the peak inductor current i_{Lp}.

For the discrete-time analysis, the clock signal initiates each switching cycle at $T(n)$ with switching period T_s divided into on-time t_1 and off-time t_2 as shown in Fig 6(b).

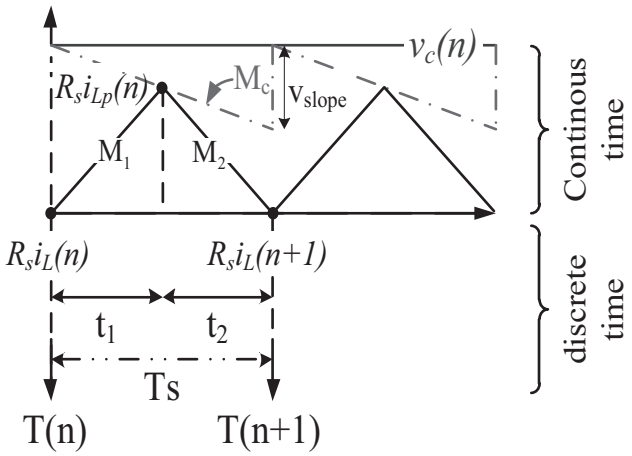
The difference equations representing the state variables inductor current (i_L) and output voltage (v_O) can be formulated from the geometry of the sensed current waveforms in Fig 6(b). The difference equation representing the discrete-time inductor current i_L at sampling instant $T(n+1)$ can be written as:

$$i_L\,(n+1) = \frac{R_s i_{Lp}\,(n) - M_2 t_2}{R_s} \tag{12}$$

The difference equation representing the discrete-time output voltage $v_O(n+1)$, can be represented as the sum of the previous output voltage $v_O(n)$ at sampling instant $(T(n))$ and the voltage difference due to the flow of charge in the output capacitor. This charge consists of the charge supplied by the inductor during t_2 and the charge drained by the load resistance during the



(a) Continuous-time domain converter waveform for PCMC



(b) Continuous-time to discrete-time domain representation

Fig. 6. Converter waveforms for PCMC with continuous-time and sampled discrete-time at clock T(n).

full switching cycle. The current during t_2 is the average current of $i_{Lp}(n)$ and $i_L(n+1)$ and hence the output voltage can be expressed as:

$$v_O\left(n+1\right) = v_O\left(n\right) + \frac{\left(i_{Lp}\left(n\right) + i_L\left(n+1\right)\right) t_2}{2C} - \frac{v_O\left(n\right) T_s}{R_L C} \tag{13}$$

In (12) and (13), it is easy to see from Fig 6(b) that:

$$R_s i_{Lp}\left(n\right) = R_s i_L\left(n\right) + t_1 M_1$$

$$t_1 = \frac{v_C\left(n\right) - R_s i_L\left(n\right)}{M_1 + M_c}$$

$$t_2 = T_s - t_1,$$

Also, from the power stage as shown in Fig 5 we know that:

$$M_1 = \frac{V_{dd}\, Rs}{L}, \quad M_2 = \frac{\left(v_O - V_{dd}\right) R_s}{L},$$

$$D' = 1 - D$$

Where D represents the duty ratio and V_{dd} is the supply voltage. In order to construct the small-signal model, (12) and (13)

are first written as a function of only $i_L(n)$, $v_C(n)$ and $v_O(n)$ as:

$$i_L(n+1) = i_L(n) - \frac{(v_O(n) - V_{dd})T_s}{L} + (v_C(n) - i_L(n)R_s)K_1 \tag{14}$$

where

$$K_1 = \frac{M_1 + M_2}{R_s(M_1 + M_c)}$$

$$v_O(n+1) = v_O(n) + \frac{R_s i_L(n) + M_1 t_1 + R_s i_L(n+1)}{2R_s C}.t_2 \tag{15}$$
$$-K_2$$

where

$$K_2 = \frac{v_O(n)T_s}{R_L C}$$

The next step involves perturbation around the steady state point which is done by applying the following substitutions:

$$i_L(n+1) \to I_L(n+1) + i_l(n+1) \tag{16}$$

$$i_L(n) \to I_L(n) + i_l(n) \tag{17}$$

$$v_C(n) \to V_C(n) + v_c(n) \tag{18}$$

$$v_O(n) \to V_O(n) + v_o(n) \tag{19}$$

$$v_O(n+1) \to V_O(n+1) + v_o(n+1) \tag{20}$$

Where $I_L(n+1)$, $I_L(n)$, $V_C(n)$, $V_O(n)$ and $V_O(n+1)$ are the DC steady state terms. By substitution of (16), (17), (18), (19) and (20) in (14) and (15) the DC, first and second order terms are obtained. For the small-signal derivation the DC terms are cancelled and the second order terms are ignored, which results in the following simplified small-signal difference equation:

$$i_l\,(n+1) = -i_l\,(n)\,k_0 - v_o\,(n)\,k_1 + \,v_c\,(n)\,k_2 \tag{21}$$

$$v_o\,(n+1) = i_l\,(n)\,k_3 + v_o\,(n)\,k_4 + v_c\,(n)\,k_5 \tag{22}$$

where

$$k_0 = \alpha = \frac{M_2 - M_c}{M_1 + M_c}$$

$$k_1 = \frac{(1-D)\,T_s}{L}, k_2 = \frac{V_{dd}}{(1-D)\,L\,(M_1 + M_c)}$$

$$k_3 = -\frac{\alpha\,D'\,Ts}{C} + \frac{M_1 L}{C\,(M_1 + M_c)\,R_L D'^2} + \frac{M_1\,(D)\,Ts}{2C\,(M_1 + M_c)}$$

$$k_4 = 1 - \frac{D'^2\,Ts^2}{2CL} - \frac{Ts}{R_L C}$$

$$k_5 = \frac{V_{dd}\ Ts\ (1 - 0.5\,D)}{CL\,(M_1 + M_c)} - \frac{V_{dd}}{C\,(M_1 + M_c)\,R_L D'^2}$$

Equation (21) and (22) are the fundamental equations for the PCMC based boost converter and can be now easily converted to state-space representation.

The independent states $(i_l\,and\,v_o)$ in the circuit contribute to the state vector $\mathbf{x}[n]$ and the independent input source (v_c) to the input vector $\mathbf{u}[n]$. Hence the general state-space model of a PCMC based boost converter can be represented as:

$$\mathbf{x}[n+1] = A\mathbf{x}[n] + B\mathbf{u}[n] \tag{23}$$

where

$$\mathbf{u}[n] = v_c(n), \quad \mathbf{x}[n] = \begin{bmatrix} i_l(n) \\ v_o(n) \end{bmatrix}$$

$$A = \begin{bmatrix} -k_0 & -k_1 \\ k_3 & k_4 \end{bmatrix},\ B = \begin{bmatrix} k_2 \\ k_5 \end{bmatrix}$$

(23) is a complete state-space representation of the circuit and the control-to-output transfer function can be found by taking the Z-transform:

$$z\mathbf{x}(z) = A\mathbf{x}(z) + B\mathbf{u}(z) \tag{24}$$

rearranging we get,

$$\frac{\mathbf{x}(z)}{\mathbf{u}(z)} = (zI - A)^{-1}B \tag{25}$$

Where I is the identity matrix. Substituting the matrices of A and B in (25) and rearranging the terms, the control-to-output discrete-time transfer function $T_{co}(z)$ can be written as:

$$T_{co}(z) = \frac{v_o(z)}{v_c(z)} = G_0 \frac{a_4 z + a_3}{a_2 z^2 + a_1 z + a_0} \tag{26}$$

where

$$G_0 = \frac{-V_{dd}}{D'^2(M_1 + M_c)}$$

$$a_4 = 2\,L\,(M_1 + M_c)\,D' + (M_1 + M_c)\,R_L\,(-2 + D)\,T_s D'^3$$

$$a_3 = (\alpha\ (M_1 + M_c)\,D' - M_1)\left(R_L T_s D'^2\,(D) + 2\,L\right)$$

$$a_2 = 2\,CD'\,LR_L\,(M_1 + M_c)$$

$$a_1 = 2D'((C(\alpha - 1)L + \frac{{T_s}^2 D'^2}{2})R_L + LT_s)(M_1 + M_c)$$

$$a_0 = -\alpha\,R_L {T_s}^2\,(M_1 + M_c)\,D'^3 + D'^2\,(D)\,R_L {T_s}^2 M_1$$

$$-2\,\alpha\ (M_1 + M_c)\,L\,(-T_s + CR_L)\,D' + 2\,LT_s M_1$$

B. Continuous-time domain representation

Equation (26) gives an accurate system representation in discrete-time domain and can be very helpful in making digital control circuits. However, for better insight into how different circuit parameters influence the behaviour of the transfer function, a continuous-time representation can be very helpful. Therefore in this section, (26) is converted to continuous-time using a second-order Padé approximation of $z = e^{sT_s}$. A first-order approximation of e^{sT_s} would not change the number of poles, and would not be able to translate the left half plane z-domain pole that describes the ringing around $f_s/2$ [26].

$$z = e^{sT_s} \approx \frac{s^2 + 6f_s s + 12{f_s}^2}{s^2 - 6f_s s + 12{f_s}^2}, \quad (T_s = \frac{1}{f_s}) \tag{27}$$

Putting (27) in (26), the continuous-time domain control-to-output transfer function $T_{co}(s)$ results in a fourth-order function with the form of :

$$T_{co}(s) = \frac{q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0}{p_4 s^4 + p_3 s^3 + p_2 s^2 + p_1 s + p_0} \tag{28}$$

The coefficients of (28) can be simplified by using the following assumptions:

$$f_s \gg \frac{1}{2\pi R_L C} \tag{29}$$

$$f_s \gg \frac{1}{2\pi\sqrt{LC}} \tag{30}$$

This means that the switching frequency is higher than the $R_L C$ and LC frequency of the power stage. This will generally be true to achieve an acceptable ripple, so (28) can be rewritten as:

$$T_{co}(s) = \frac{k'\left(c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s + c_0\right)}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{31}$$

where

$$k' = -2V_{dd}$$

$$c_4 = -{T_s}^4 {D'}^2 R_L$$

$$c_3 = 6\,{D'}^2 D R_L {T_s}^3 + 12\,L{T_s}^2$$

$$c_2 = -72\,T_s\left(1/2\,R_L\left(-1/3 + D\right){D'}^2 T_s + L\right)$$

$$c_1 = 144\,L + 72\,R_L {D'}^2 T_s D$$

$$c_0 = -144\,{D'}^2 R_L$$

$$b_4 = 2{T_s}^4\left(\frac{{D'}^3 R_L T_s (M_1 + M_c)}{2} + \right.$$

$$\left. LD'(1+\alpha)(M_1 + M_c) + LM_1\right)$$

$$b_3 = 24CD'LR_LT_s(M_1 + M_c)$$

$$b_2 = (1-\alpha)(144CD'LR_LT_s(M_1 + M_c))$$

$$b_1 = (288CD'LR_L(1+\alpha)(M_1 + M_c)) = 288V_{dd}R_sCR_L$$

$$b_0 = \frac{144T_s}{L}(D'^3R_L(V_{dd}R_s + 2M_cL) + 4LV_{dd}\frac{R_s}{T_s})$$

As can be seen in (31), the conversion to continuous-time results in extra poles and zeros. Often the transfer function contains many poles and zeros, having a single dominant pole or zero. Similarly for practical power converters to work, the dominant pole (ω_{p1}) needs to be at a much lower frequency than the other poles. Hence in this case, dominant pole approximation as explained in [27] is useful to extract the low frequency pole.

If a circuit has n number of poles and m number of zeros, the transfer function T(s) can be expressed generally as:

$$T(s) = \frac{a_0 + a_1s + a_2s^2 + a_3s^3 + \cdots + a_ms^m}{b_0 + b_1s + b_2s^2 + b_3s^3 + \cdots + b_ns^n} \tag{32}$$

If a system represented by (32) is known to have a dominant pole located at much lower frequency than the other (n-1) poles, the higher frequency poles are neglected at lower frequencies, resulting in a first order transfer function. Then, the dominant pole in (31) can be calculated as:

$$\omega_{p1} = \frac{b_0}{b_1},\ where \quad \omega_{p1} \ll \omega_{p2}, \omega_{p3}, ... \tag{33}$$

At higher frequencies, b_1s then dominates b_0, so the complexity of the denominator in (31) can be reduced. The same technique is used on the numerator of (31) to extract the dominant zero. Subsequently, poles and zeros above $\frac{f_s}{2}$ are neglected, which leads to the final form:

$$T_{co}(s) = G_0\frac{1 - \frac{s}{\omega_{rhpz}}}{(1 + \frac{s}{\omega_p})(s^2 + 6f_s s\frac{(1-\alpha)}{(1+\alpha)} + 12{f_s}^2)} \tag{34}$$

where

$$G_0 = \frac{24L{f_s}^3R_LD'V_{dd}}{D'^3R_LV_{dd}R_s + 2D'^3R_LM_cL + 4f_sLV_{dd}R_s}$$

$$\omega_{rhpz} = \frac{D'^2R_L}{L}$$

$$\omega_p = (1-D)^3\frac{(\frac{M_c}{M_1} + 0.5)}{LCf_s} + \frac{2}{R_LC}$$

Where G_0 is the DC gain, ω_{rhpz} is the right-half plane zero frequency, the second order term describes the subharmonic poles and ω_p is the dominant pole frequency. The model presented in (34) is not only comprehensible and accurate but can directly be applied to capacitive loads. So for a purely capacitive loads ($R_L \to \infty$) the second term of ω_p is zero, leaving:

$$\omega_p = (1-D)^3\frac{(\frac{M_c}{M_1} + 0.5)}{LCf_s} \tag{35}$$

IV. Simulation Results

In order to validate the model in (34), the results are first compared to simulations in SIMPLIS with circuit parameters listed in table I.

A PCMC based boost converter running in CCM is simulated in SIMPLIS with an RC load ($R_L = 50\Omega$, $C = 10\mu$F) and other parameters as listed in table I, and the control-to-output transfer function is plotted in Fig 7. The results from (34) match well with the simulation for both high and low frequencies. The same model is then used for a purely capacitive load

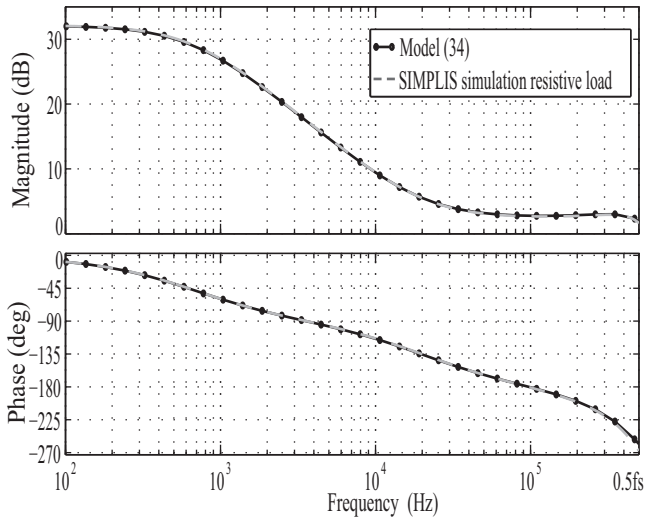


Fig. 7. Control-to-output transfer $T_{co}(s)$ according to model (34) and SIMPLIS simulation for R_L=50Ω, C=10μF

($R_L \to \infty$) and the results are compared with the simulations in SIMPLIS in Fig 8. Again, the results match well with the simulation.

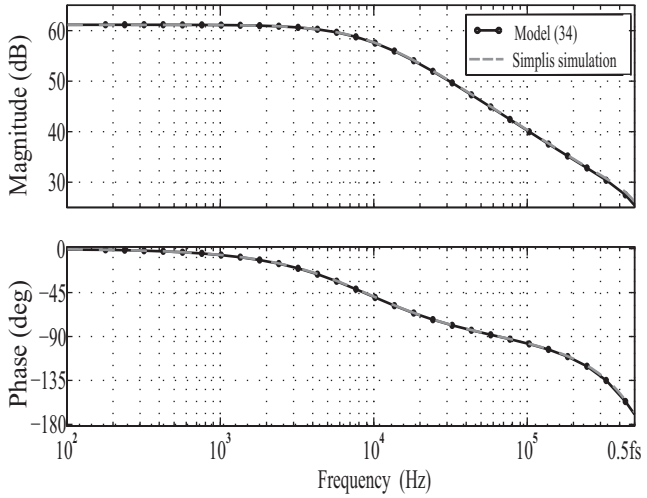


Fig. 8. Control-to-output transfer $T_{co}(s)$ according to model (34) and SIMPLIS simulation for capacitive load ($R_L = \infty$, C=26nF).

The dominant pole location in (34) is strongly influenced by the choice of duty cycle, considering other parameters remain constant. It is interesting to observe the effect of dominant pole movement for wide duty cycle variations as shown in Fig 9. For purely capacitive loads, the dominant pole deviation is significant and cannot be ignored. In order to ensure the validity

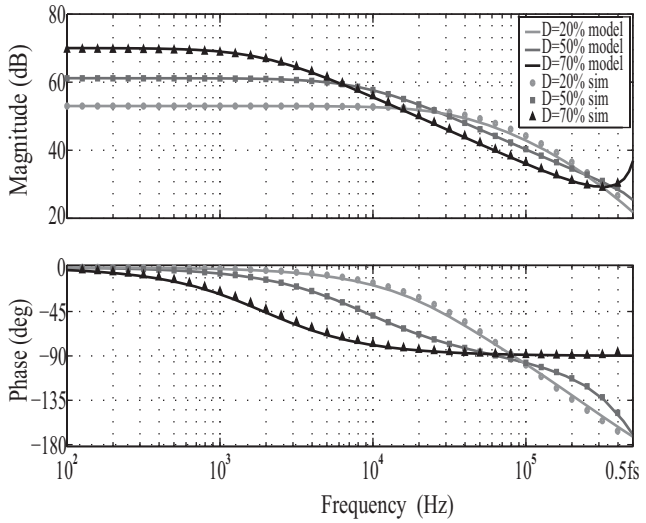


Fig. 9. Effect of duty cycle variation on the dominant pole location for a capacitive load

of these simulation and modeling results, the model is also verified by experimental verification for a capacitive load in the next section.

V. Experimental Verification

The experimental results for a PCMC based boost converter are only verified for a capacitive load due to the focus of the project involved. The simulation setup above demonstrates the real application area, however as the original circuit is not yet realised, an existing boost converter board is used to verify the model and simulation results. The schematic of the setup is shown in Fig 10. The LM5122EVM-1PH synchronous boost controller evaluation module (shown in Fig 11) is used in Forced

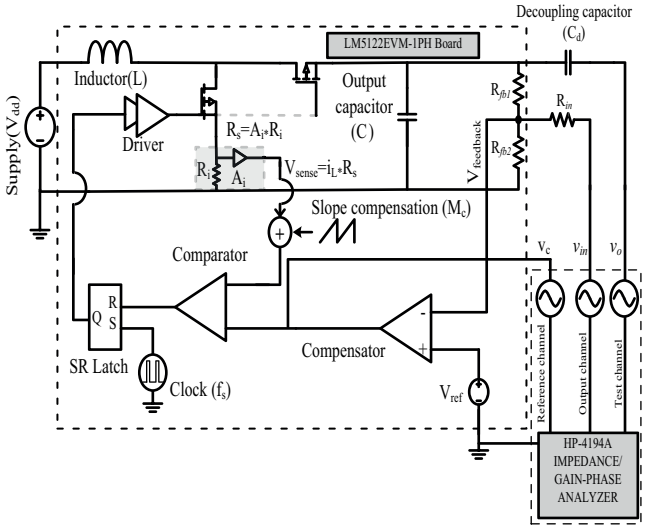


Fig. 10. Measurement schematic of a peak current-mode control based bi-directional boost converter with capacitive load (370μF)

PWM mode for these measurements along with a gain-phase analyzer (HP-4194A). The circuit parameters are listed in table II.

A capacitor in a practical circuit has an equivalent series resistance (ESR). For practical converters, the ESR of the capacitor

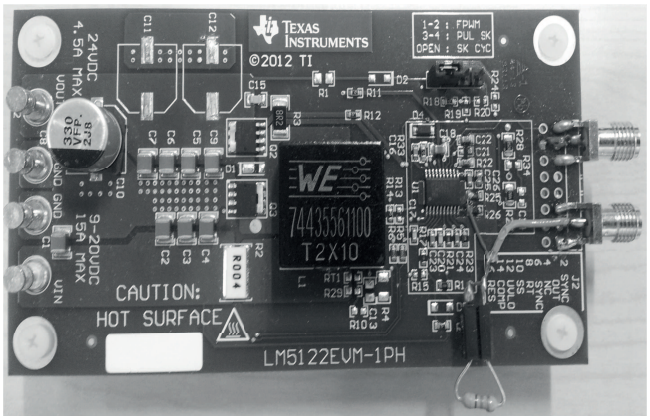


Fig. 11. Modified LM5122EVM-1PH synchronous boost controller evaluation module

TABLE II
CIRCUIT PARAMETERS

Parameters	Values
Duty ratio (D)	0.5
Inductor (L)	10 μH
Current sense gain($R_s = R_i \cdot A_i$)	4mΩ*10
Supply voltage (V_{dd})	12V
Switching frequency (f_s)	250kHz
Control voltage (Vc)	168mV
Slope compensation (peak-peak)	270mV
Output capacitance (C)	370μF
Load resistance for capacitive load (R_L)	∞
Decoupling capacitor (C_d)	22nF
Input resistance (R_{in})	47kΩ

is much smaller than the load resistance. Therefore the ESR of the capacitor only adds an extra zero in the transfer function and doesn't change the DC gain and the location of the dominant and subharmonic poles. Hence the capacitor's ESR was ignored in the main analysis as well as in Fig 3 and 4. However for the experimental verification, ESR is present in the circuit and to validate the effect of the ESR-zero, a small resistance of $55m\Omega$ is added to the capacitance in simulation and the results are shown in Fig 12. Similarly, to accommodate the effect of ESR in the model, a real zero can be added to final model with the following expression:

$$\omega_{zero} = \frac{1}{R_{esr} \cdot C} \tag{36}$$

The experimental verification of the modeling is done using a testbed which is not designed to operate under such load (370μF) conditions. We used less output capacitance in order to be able to show the low frequency pole. As a result, the test board of the boost converter does not operate properly above $0.2f_s$ signal frequency. Although the board is originally designed to operate under wide duty ratio variation, reducing the output capacitor to a low value limits stable operation to around a duty ratio of 0.5. Therefore the measurements are only performed for a duty ratio of 0.5. The results show that the model accurately predicts the DC gain, dominant pole and subharmonic poles. The measurement results of the control-to-output transfer function match well with the model at low frequencies, with some slight deviation at high frequencies, likely caused by measurement artifacts.

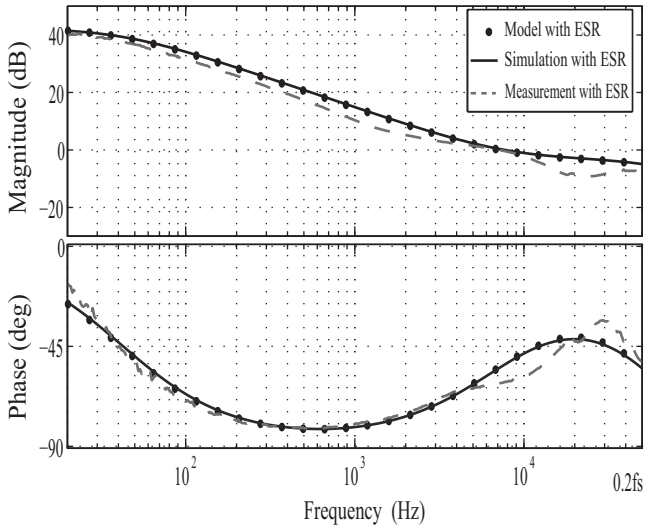


Fig. 12. Comparison control-to-output transfer $T_{co}(s)$ with simulation, measurement and model ($R_L \to \infty$).

VI. Conclusion

A new modeling approach to derive the control-to-output transfer function for peak current-mode controlled DC-DC boost converter operating in CCM is proposed. The main advantage of the proposed approach is its straightforwardness and accuracy. The power stage transfer including inductor current-to-output voltage and duty cycle-to-output voltage need not to be derived.

The location of the dominant pole and how it is affected by circuit parameters can help to design an accurate compensator, reduce static error and distortion at the output, especially in the case where the dominant pole moves to higher frequencies. With dynamic signals, the operating range of the duty cycle is significant and hence care must be taken for the design of slope compensation, selection of switching frequency and feedback compensation.

The control-to-output voltage transfer function derived here agrees very well with the simulation and measurement results. The modeling approach in this paper concentrates on a PCMC based boost converter, but the method can also be applied to buck or buck-boost converter topologies.

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