Modelling and control of DC-DC converters

This tutorial article shows how the widely used analysis techniques of averaging and linearisation are applied to the buck or step-down DC-DC converter to obtain simple equations which may then be used for control design. Three common control methods are described. Their principal characteristics are illustrated using Matlab and the Simulink block diagram system along with experimental results. The analysis procedures described may be applied directly to other DC-DC converters and the principles may be extended to more complex power electronic systems.

by A. J. Forsyth and S. V. Mollov

DC-DC converters are some of the simplest power electronic circuits. They are widely used in the power supply equipment for most electronic instruments and also in specialised high-power applications such as battery charging, plating and welding. In addition to a controllable and theoretically lossless DC voltage transformation, DC-DC converter circuits may also provide voltage isolation through the incorporation of a small high-frequency transformer. The wide variety of circuit topologies ranges from the single-transistor buck, boost and buck/boost converters to complex configurations comprising two or four devices and employing soft-switching or resonant techniques to control the switching losses.[1,2] However, similar methods of analysis and control are applied to many of these converters.

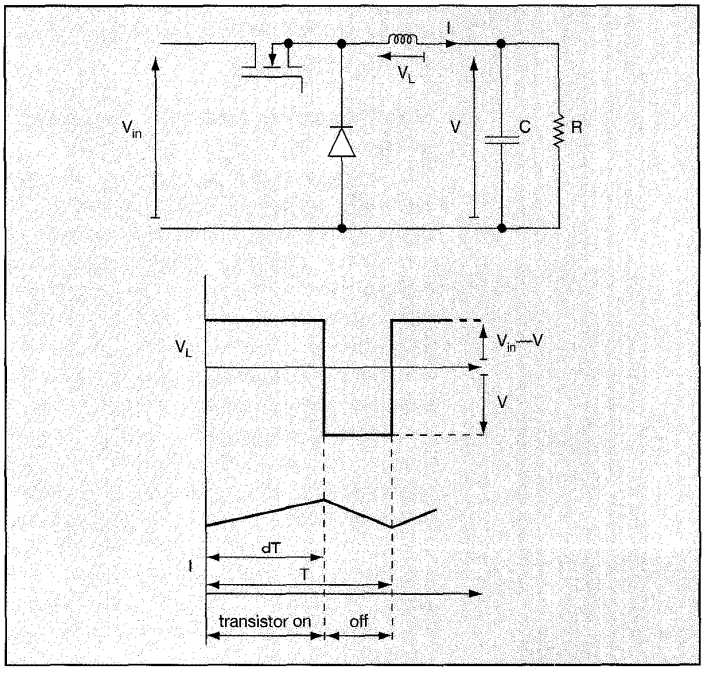
Buck converter

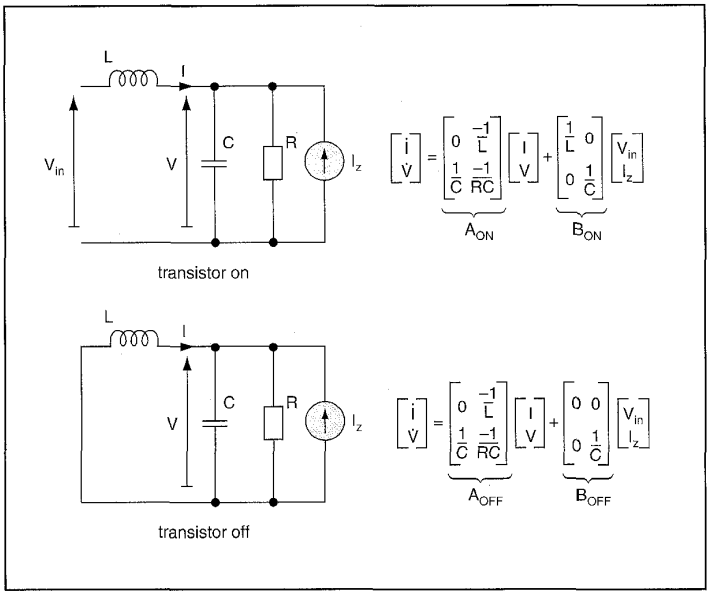
Fig. 1 shows a circuit diagram of a buck converter along with idealised waveforms for the inductor voltage and current. The transistor operates at a fixed frequency, period T, and with an on-time to period ratio or duty-ratio d. The inductor current is assumed to be continuous, the circuit components are lossless and the output capacitor ripple voltage is considered negligible. The relationship between steady-state output voltage and duty-ratio is obtained by equating the positive and negative inductor volt-seconds in a switching cycle. The volt-seconds must balance in steady-state operation:

$$(V_{in} - V)dT = V(1 - d)T$$
$$\Rightarrow V = dV_{in} \quad (1)$$

Since the value of d lies between 0 and 1, the converter output voltage must be less than or equal to the input voltage.

1 Buck DC-DC converter and idealised waveforms





2 Circuit configurations of the buck converter assuming continuous inductor current

The usual requirement of a control system for the converter is to maintain the output voltage constant irrespective of variations in the DC source voltage V_{in} and the load current. According to the steady-state equation for the output voltage (eqn. 1), V is independent of load conditions. However, as we will see, load changes affect the output voltage transiently, possibly causing significant deviations from the steady-state level. Furthermore, in a practical system circuit losses introduce an output voltage dependency on steady-state load current which must be compensated for by the control system.

Modelling power electronic converters by averaging

The inherent switching operation of power electronic converters results in the circuit components being connected together in periodically changing configurations, each configuration being described by a separate set of equations. The transient analysis and control design for converters is therefore difficult since a number of equations must be solved in sequence. The technique of averaging provides a solution to this problem. A single equation may be formed to described the converter approximately over a number of switching cycles by simply taking a linearly weighted average of the separate equations for each switched configuration of the converter. State-space averaging[1-4] is the most common averaging technique and is used here to model the buck converter.

Fig. 2 shows the two circuit configurations of the buck converter corresponding to the two states of the transistor. A third configuration occurs if the inductor current becomes discontinuous but is not considered here. In order to provide a facility in the model for examining the response of the converter to load changes, a current generator I_z is added in parallel with the load resistor in Fig. 2. The Figure also shows the equations for each circuit configuration expressed in standard state-space form. The inductor current I and output capacitor voltage V are the two elements of the state vector $\boldsymbol{x}$, whilst the input vector $\boldsymbol{u}$ has elements V_{in} and I_z.

The state-space averaged model of the converter is formed by taking a weighted average of the equations in Fig. 2, and may be expressed as:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{2}$$

where $A = dA_{ON} + (1 - d)A_{OFF}$

and $B = dB_{ON} + (1 - d)B_{OFF}$

The averaged matrices for the buck converter are then

$$A = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \qquad B = \begin{bmatrix} \frac{d}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}$$

Eqn. 2 approximates the behaviour of the converter over many cycles, but the averaging process has removed all information abut the switching frequency ripple component of the variables. For the averaging approximation to be valid two main conditions must be satisfied:[3] first the state variables must evolve in an approximately linear manner in the two circuit configurations, and second the switching frequency ripple component of the state variables must be small in comparison with the average component. Both these conditions are usually satisfied in simple DC-DC converters.

The control input to the converter, the duty-ratio, appears within the $\boldsymbol{B}$ matrix of the averaged model (eqn. 2) rather than as an element in the input vector. The averaged model is therefore time varying and difficult to solve. To simplify the model, eqn. 2 is linearised by considering small variations in the variables. Each variable is written as the sum of a steady-

state or DC component and a small-signal or AC component, denoted by ~, i.e.

$$x = x + \tilde{x},\ u = u + \tilde{u} \text{ and } d = d + \tilde{d}$$

where $\tilde{x} << x$, $\tilde{u} << u$ and $\tilde{d} << d$

These expressions for the variables are then substituted into eqn. 2, the equation is multiplied out and products of small-signal quantities are neglected. After subtracting the DC components of the variables the following linear equation results which relates small changes in the variables:

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} + E\tilde{d} \qquad (3)$$

where the A and B matrices are given by the expressions in eqn. 2 and

$$E = (A_{ON} - A_{OFF})\,x + (B_{ON} - B_{OFF})u$$

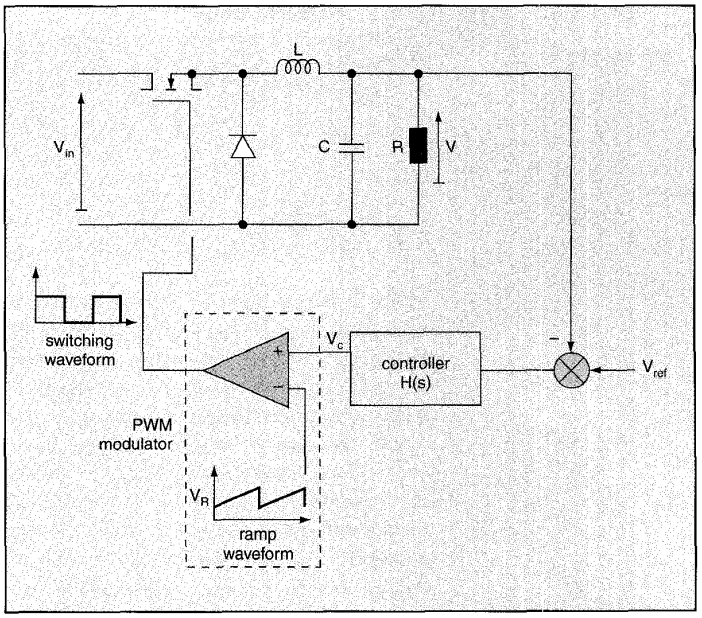
The E matrix for the buck converter is given by:

$$E = \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}$$

Standard linear systems techniques may then be used to obtain algebraic expressions for the converter transfer functions, allowing control loop design and the examination of closed loop characteristics. Instead of taking this mathematical approach, the Simulink block diagram system is used here to calculate and plot the converter transfer functions.

Single-loop control

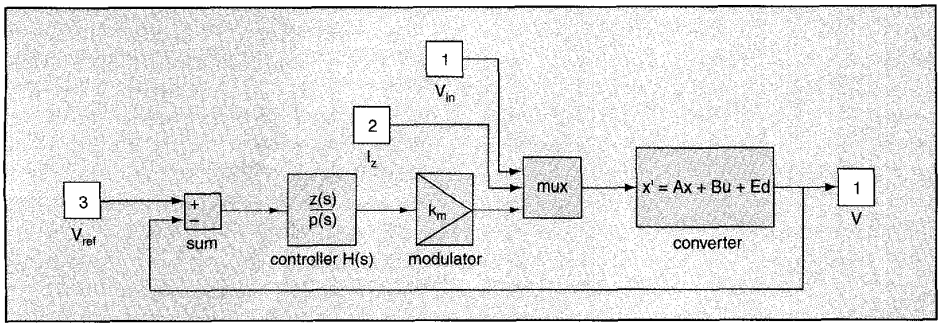
The output voltage is regulated by closing a feedback loop between the output voltage and duty-ratio signal (Fig. 3). The output voltage is compared with a constant reference signal V_{ref} to form the error, which is then passed through the control transfer function $H(s)$ to generate a control signal V_c; finally the PWM modulator converts the control signal into the transistor drive waveform.



3 Single-loop control

The negative feedback summation and the control transfer function are normally implemented using a single op-amp whilst the PWM modulator is formed by a comparator and ramp generator (Fig. 3). Dedicated integrated circuits are available for the control of DC-DC converters, they typically comprise a control amplifier, modulator circuitry, a latch for the comparator output to prevent 'switch bounce', and also housekeeping functions such as current limit, shutdown and soft-start. Simple analogue circuit-based control systems such as this are the most appropriate for many DC-DC converter applications due to their low cost and high speed.

Fig. 4 shows the Simulink block diagram of the converter system. The converter is represented by the small-signal state-space averaged model (eqn. 3), the elements in the matrices being evaluated using the parameter



4 Simulink model of converter with single-loop control

Table 1 Parameter values

parameter	value
V_{in}	24 V
V	12 V
R	11 Ω
L	335 μH
C	10 μF
T	21 μs

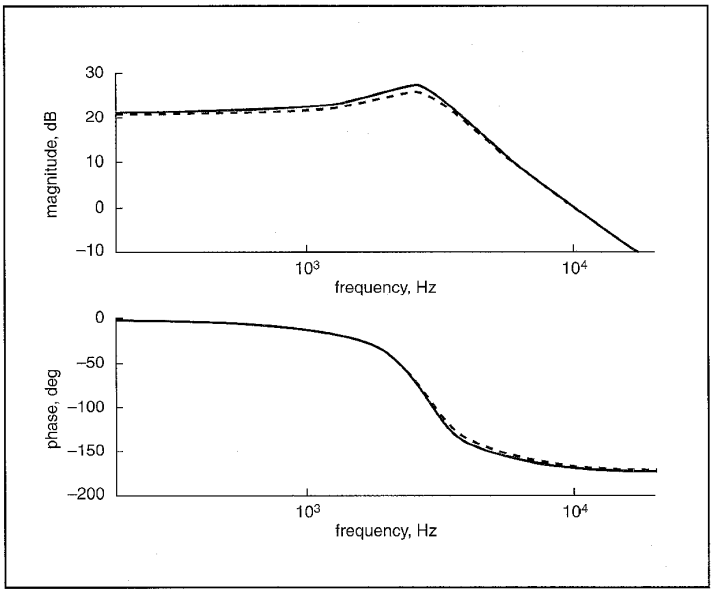
values listed in Table 1. The parameters are taken from a prototype system which is used below to provide supporting experimental results. The small-signal source voltage and load current are shown as external inputs whilst the duty-ratio is determined by the control loop. The mux block simply combines the three signals V_{in}, I_z and d into vector form for the state-space equations. There is a single output from the state space equation block, the output voltage V. The PWM modulator is represented by a small-signal gain k_m which is determined below.

Assuming that the peak and valley levels of the ramp waveform are denoted by V_p and V_v, respectively, then the duty ratio d is given in terms of the control voltage V_c by:

$$d = \frac{V_c - V_v}{V_p - V_v} \tag{4}$$

The small-signal gain of the modulator is then

$$k_m = \frac{\partial d}{\partial V_c} = \frac{1}{V_p - V_v} \tag{5}$$



5 Open-loop $\tilde{V}/\tilde{V}_c$ frequency response plot (– prediction, ---measurement)

the value of k_m in the prototype was 0·5.

The controller transfer function $H(s)$ is chosen to have an integral characteristic at low frequency in order to ensure zero steady-state error. A compensation term is added at higher frequency to provide a satisfactory crossover frequency and stability margin. The crossover frequency of the control loop is typically restricted to around one-tenth of the switching frequency since this usually provides an acceptable compromise between speed of response and avoiding switching frequency related instabilities.

Fig. 5 shows the open-loop control-to-output frequency response $\tilde{V}/\tilde{V}_c$ for the converter. The solid line represents data generated from Simulink by removing the control loop shown in Fig. 4. The broken line shows measured data from the prototype system. The measurement was made using a network analyser; the oscillator output from the analyser was superimposed onto the modulator control signal V_c using a wideband signal transformer. The resulting small-signal disturbance in the converter output voltage was measured by the analyser and the frequency response plotted. There is close correspondence between the two sets of data up to the maximum frequency plotted, 20 kHz, illustrating the accuracy of the model. The small discrepancy is due to the absence of circuit losses from the model. Averaged models are typically accurate up to around one-third of the switching frequency. The frequency response has the familiar form of a second-order transfer function with under-damped poles at 2·5 kHz.

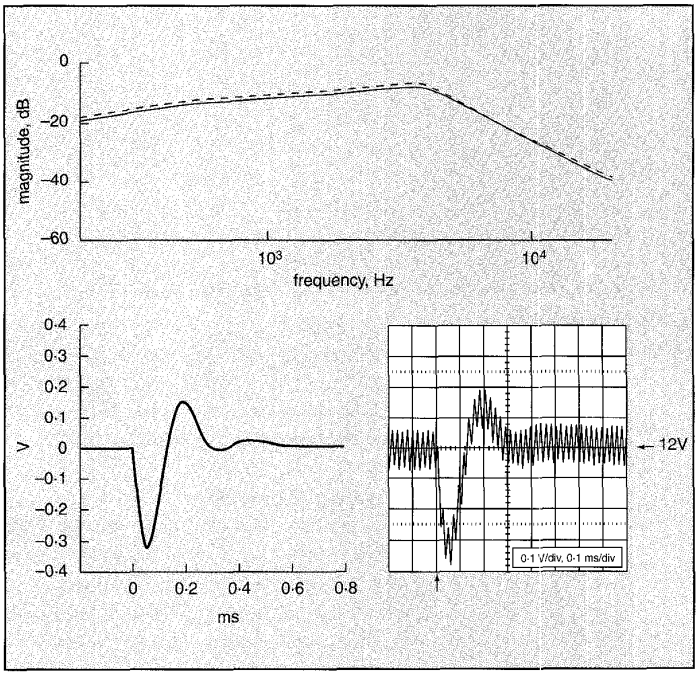
In order to achieve a crossover frequency of around 5kHz (one-tenth the switching frequency) the controller transfer function $H(s)$ was designed to be

$$H(s) = \frac{0{\cdot}24\ (s + 10\text{k})^2}{s(s + 60\text{k})} \tag{6}$$

The two zeros are placed at 10krads^{-1}, just below the converter pole frequency and a high frequency pole is placed at 60krads^{-1}, approximately twice the target crossover frequency. The magnitude of $H(s)$ was chosen to give a crossover frequency of 4kHz, the phase margin being 65°.

Fig. 6 shows the closed-loop performance of the system. The magnitude of the DC source voltage to output voltage transfer function $\tilde{V}/\tilde{V}_{in}$ is plotted as a frequency response; the solid line

is from the Simulink model and the broken line represents measured data. There is at least 7dB attenuation of input voltage disturbances across the entire frequency range. Fig. 6 also shows a predicted and measured time domain response of the output voltage to a 0·12 A step increase in load current. The prediction from the model has no switching frequency ripple or steady-state component. In addition to being underdamped, the response also has a slowly decaying component which arises due to the two zeros in $H(s)$ and the relatively low loop gain at low frequency.



6 Closed-loop performance – single-loop control. Top: $\tilde{V}/\tilde{V}_{in}$ (– prediction, --- measurement); Bottom: output response to 0·12A step increase in load (prediction on left, measurement on right)

Input voltage feedforward

Input voltage feedforward increases the immunity of the converter output voltage to disturbances in the DC input voltage. This is accomplished by making the peak value of the PWM modulator ramp waveform V_p proportional to the DC input voltage V_{in}. An increase in the DC source voltage will then increase the slope of the PWM ramp and lead to an almost instantaneous reduction in transistor duty-ratio, thereby compensating for the increase in source voltage and reducing the resultant disturbance in the converter output voltage.

A linearised small-signal representation for the PWM modulator is again determined from the duty-ratio equation (eqn. 4), but with the peak value of the ramp voltage V_p expressed as a linear function of V_{in}, $V_p = k_f V_{in}$:

$$d = \frac{V_c - V_v}{k_f V_{in} - V_v} \tag{7}$$

A linear expression relating small changes in duty-ratio $\tilde{d}$ to small changes in input voltage and control voltage, $\tilde{V}_{in}$ and $\tilde{V}_c$, respectively, is obtained by taking the first-order terms in the Taylor series for $\tilde{d}$:

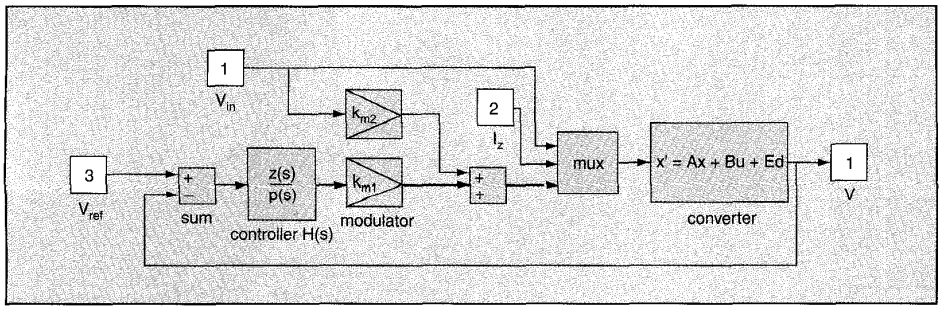
$$\tilde{d} = \frac{\partial d}{\partial V_c}\tilde{V}_c + \frac{\partial d}{\partial V_{in}}\tilde{V}_{in} = k_{m1}\tilde{V}_c + k_{m2}\tilde{V}_{in} \tag{8}$$

Expressions for the constants k_{m1} and k_{m2} are obtained by undertaking the partial differentiation of eqn. 7:

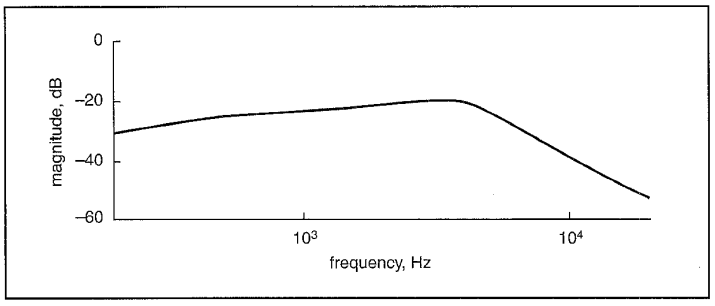
$$k_{m1} = \frac{1}{k_f V_{in} - V_v} \qquad k_{m2} = \frac{-k_f (V_c - V_v)}{(k_f V_{in} - V_v)^2}$$

A simulink model for the system is shown in Fig. 7. The converter is represented as before by the small-signal state-space averaged model (eqn. 3); the modulator is represented by eqn. 8; an output voltage feedback loop is also shown.

The addition of the feedforward does not affect the control-to-output transfer function of the converter; therefore the control loop design is identical to that described in the previous section, the controller transfer function $H(s)$ being given by eqn. 6. As a result the output voltage transient due to a step load change is identical to that shown in Fig. 6. However, an improvement is seen in the source-to-output



7 Simulink model of feedforward control



8 $\tilde{V}/\tilde{V}_{in}$ from Simulink – feedforward control

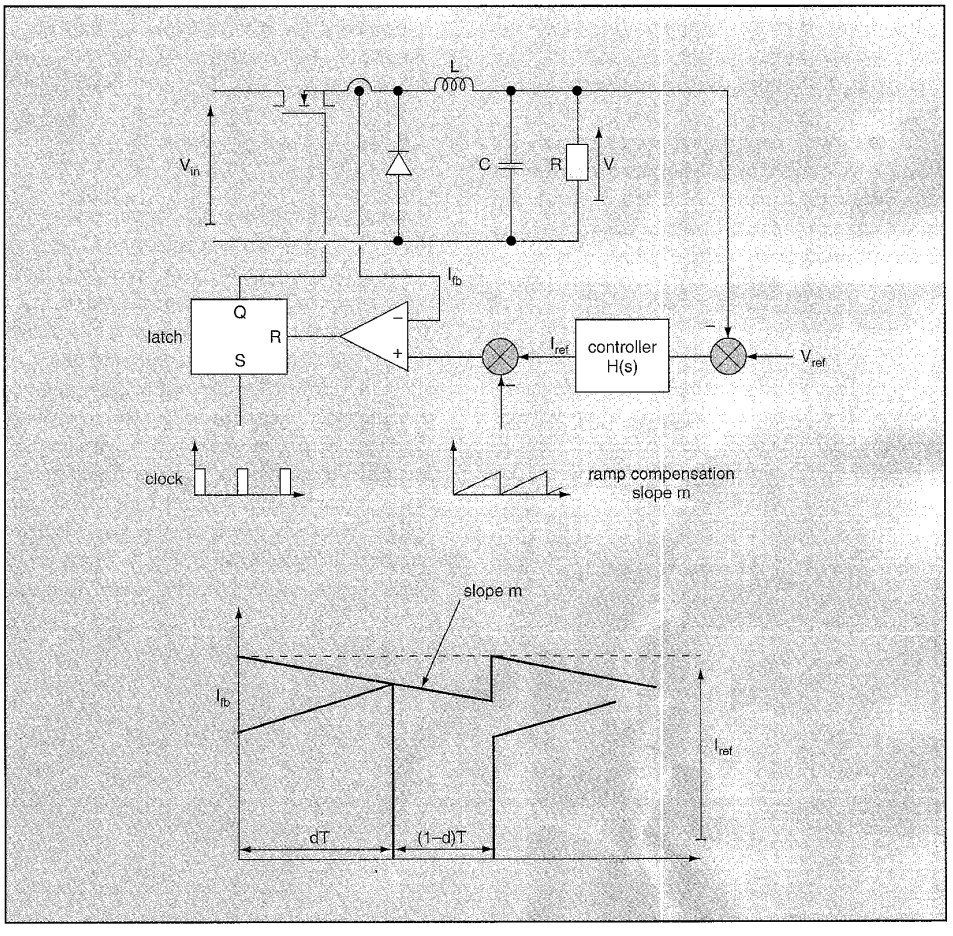
voltage frequency response, the Simulink prediction is shown in Fig. 8 where k_f was taken to be 0·1 and V_v = 0·5 V. The magnitude is reduced by over 10 dB across the full frequency range compared with the results in Fig. 6.

Current-mode control

In this control method[2,4,5] (Fig. 9), the PWM modulator is replaced by a transistor current feedback loop. The sketched waveform of the feedback current signal I_{fb} (Fig. 9) illustrates the operation of the control loop. The transistor is switched on at the start of each cycle by a clock pulse which sets the output of the latch. The transistor current rises linearly while the device is conducting. The current is fed back as signal I_{fb} and is compared with a reference signal. When I_{fb} is equal to the reference the comparator output switches low, resetting the latch and turning the transistor off.

The reference signal for the comparator is formed by an output voltage feedback loop, but the signal produced by the control transfer function I_{ref} is modified by subtracting a ramp waveform of slope m which is synchronised with the clock. The ramp is necessary to prevent switching frequency related instabilities.[4,5]

By using the transistor current to determine the turn-off instant, this control method inherently provides a current limit and protection function for the power circuit. Also, the technique provides an inherent source voltage feedforward function; an increase in the source voltage causes the transistor current to



9 Current-mode control

rise more rapidly, reaching the reference level earlier and therefore reducing the duty-ratio almost immediately. Furthermore, the control method simplifies the design of the controller since the control-to-output transfer function for the converter becomes first-order dominated; this is demonstrated below.

A small-signal representation of the current control loop is formed by considering the inductor current waveform under transient conditions (Fig. 10). The average inductor current across the switching cycle may be expressed as

$$I_{avg} = I_p - \frac{g_1 d^2 T}{2} - \frac{g_2 (1-d)^2 T}{2} \quad (9)$$

where I_p is the peak value of the current, g_1 and g_2 are the rising and falling slopes of the waveform.

The current control loop gives the relation

$$R_s I_p = I_{ref} - mdT \quad (10)$$

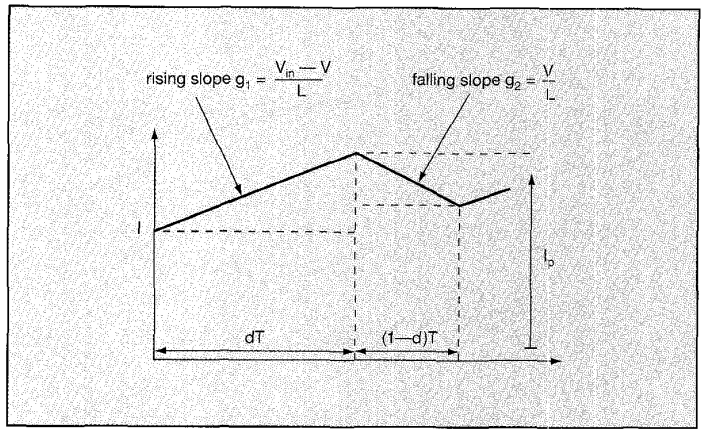
where R_s is the 'gain' of the current feedback transducer.

Eliminating g_1 and g_2 from eqn. 9 using the expressions in Fig. 10, and eliminating I_p using eqn. 10:

$$I_{avg} = \frac{I_{ref}}{R_s} - \frac{mdT}{R_s}\frac{d^2T}{2}\left[\frac{V_{in}-V}{L}\right] - \frac{(1-d)^2 T}{2}\left[\frac{V}{L}\right] \quad (11)$$

A linearised small-signal relation between the variables is obtained by taking the first-order terms in a Taylor series expansion of I_{avg}:

$$\tilde{I}_{avg} = \frac{\partial I_{avg}}{\partial I_{ref}}\tilde{I}_{ref} + \frac{\partial I_{avg}}{\partial d}\tilde{d} + \frac{\partial I_{avg}}{\partial V_{in}}\tilde{V}_{in} + \frac{\partial I_{avg}}{\partial V}\tilde{V} \quad (12)$$



10 Inductor current under transient conditions

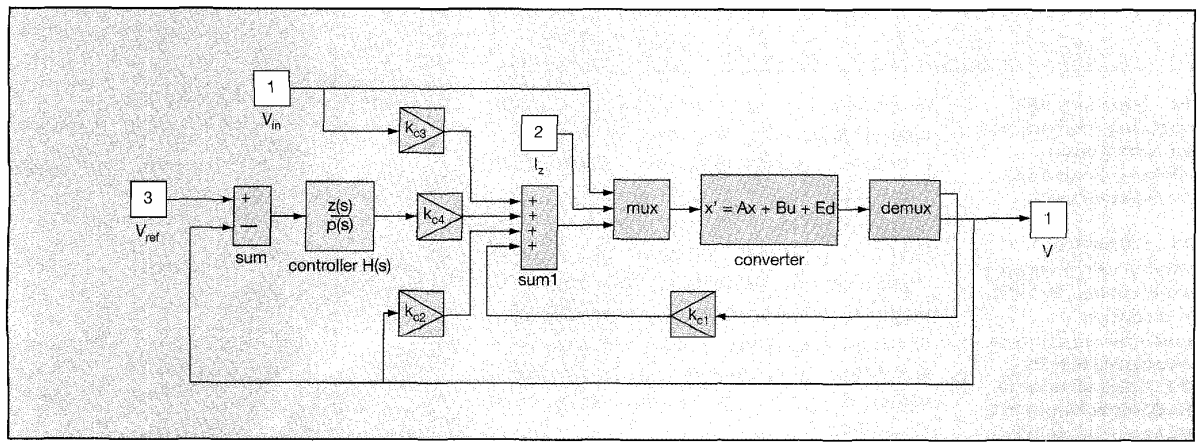
carrying out the partial differentiation and re-arranging to give an expression for $\tilde{d}$

$$\tilde{d} = -\frac{R_s}{mT}\tilde{I}_{avg} + \frac{R_s(2d-1)}{2Lm}\tilde{V} - \frac{R_s d^2}{2Lm}\tilde{V}_{in} + \frac{1}{mT}\tilde{I}_{ref} \quad (13)$$

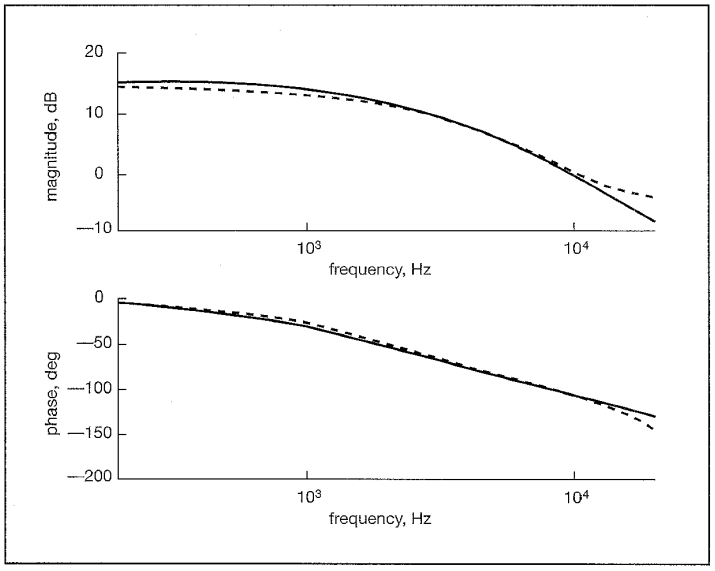
$$= k_{c1}\tilde{I}_{avg} + k_{c2}\tilde{V} + k_{c3}\tilde{V}_{in} + k_{c4}\tilde{I}_{ref}$$

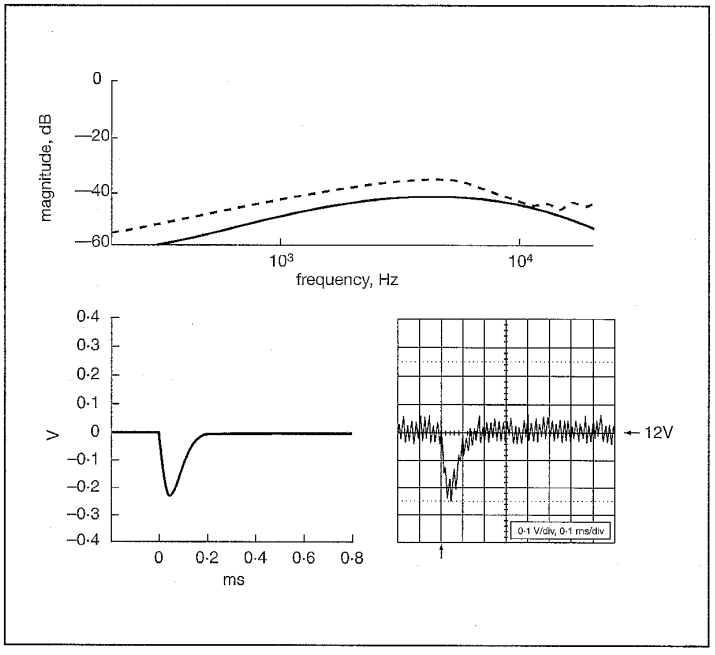
The negative term k_{c3} represents the source voltage feedforward effect of current-mode control. Fig. 11 shows a Simulink block diagram of the system. The controller is modelled as before using the small-signal state-space averaged equations (eqn. 3) and the current control loop is represented by eqn. 13. The parameters listed in Table 1 are again used with current feedback gain R_s = 1·5 Ω and m = 3·8 × 10^4 V/s. The output from the converter block is defined as the state vector, and the demux block separates the state vector into its elements.

Fig. 12 shows the predicted and measured control-to-output transfer function of the converter and current control loop, $\tilde{V}/\tilde{I}_{ref}$, the prediction in solid lines and the measurement



11 Simulink model of current-mode control





12 Open-loop $\tilde{V}/\tilde{I}_{ref}$ frequency response plot for current-mode control (—prediction, --- measurement)

13 Closed-loop performance – current-mode control. Top: $\tilde{V}/\tilde{V}_{in}$ (—prediction, --- measurement); Bottom: output response to 0·12A step increase in load (prediction on left, measurement on right)

in broken lines. As a result of the current control loop the response is first-order dominated rather than the second-order characteristic of the converter alone (Fig. 5).

The controller in the voltage feedback loop $H(s)$ is designed to have an integral characteristic at low frequency and a zero at 20 krads^{-1} to cancel the converter pole. The low-frequency magnitude of $H(s)$ was chosen to give a cross-over frequency of 5 kHz, the phase margin being 65°. Eqn. 14 gives the transfer function for $H(s)$:

$$H(s) = 0{\cdot}45\ \frac{(s + 20\text{k})}{s} \qquad (14)$$

The upper plot in Fig. 13 shows the closed-loop source to output voltage response $\tilde{V}/\tilde{V}_{in}$ for the system, the solid line shows the prediction and the broken line the measurement. Compared with the single-loop control, the attenuation of source voltage disturbances is increased by at least 30 dB, confirming the inherent source voltage feed forward characteristics of current mode control. The correspondence between measurement and prediction is not as close as before; this is because small errors in the measurement of the current control loop parameters have a large influence on the source to output response. Fig. 13 also shows the predicted and measured output response due to a 0·12A step increase in load. A rapid and well-damped response is seen.

Conclusion

The tutorial has shown how averaging and linearisation techniques may be used to obtain linear transfer functions for power electronic systems, specifically DC-DC converters. Linear system design techniques may then be used to undertake controller design and examine closed-loop performance. Three commonly used control methods for the buck DC-DC converter are described and compared. Current-mode control is seen to offer superior performance in both the rejection of source voltage disturbances and the response to load transients.

Further reading

1 MOHAN, N., UNDELAND, T.M., and ROBBINS, W. P.: 'Power electronics: converters, applications and design' (Wiley, 1995, 2nd Edn.)
2 KASSAKIAN, J. G., SCHLECHT, M. F., and VERGHESE, G. C.: 'Principles of power electronics' (Addison Wesley, 1991)
3 MIDDLEBROOK, R. D., and CUK, S.: 'A general unified approach to modelling switching converter power stages', *International Journal of Electronics*, 1977, 42, (6), pp.521–550
4 MITCHELL, D. M.: 'DC-DC switching regulator analysis' (McGraw Hill, 1988)
5 VERGHESE, G. C., BRUZOS, C. A. and MAHABIR, K. N.: 'Averaged and sampled-data models for current mode control: a re-examination', IEEE Power Electronics Specialists Conference, 1989, pp.484–491

The authors are with the School of Electronic & Electrical Engineering, University of Birmingham, Edgbaston, Birmingham B15 2TT, UK.