A 1 mW 71.5 dB SNDR 50 MS/s 13 bit Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC

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***Abstract*—This paper presents a 13 bit 50 MS/s fully differential ring amplifier based SAR-assisted pipeline ADC, implemented in 65 nm CMOS. We introduce a new fully differential ring amplifier, which solves the problems of single-ended ring amplifiers while maintaining the benefits of high gain, fast slew based charging and an almost rail-to-rail output swing. We implement a switched-capacitor (SC) inter-stage residue amplifier that uses this new fully differential ring amplifier to give accurate amplification without calibration. In addition, a new floated detect-and-skip (FDAS) capacitive DAC (CDAC) switching method reduces the switching energy and improves linearity of first-stage CDAC. With these techniques, the prototype ADC achieves measured SNDR, SNR, and SFDR of 70.9 dB (11.5b), 71.3 dB and 84.6 dB, respectively, with a Nyquist frequency input. The prototype achieves 13 bit linearity without calibration and consumes 1 mW. This measured performance is equivalent to Walden and Schreier FoMs of 6.9 fJ/conversion·step and 174.9 dB, respectively.**

***Index Terms*—ADC, analog to digital converter, energy efficient ADC, fully differential ring amplifier, low power ADC, pipeline ADC, pipelined SAR ADC, SAR ADC, SAR-assisted pipeline ADC, switched capacitor.**

I. Introduction

THE SAR-assisted pipeline ADC architecture [1], [2] is an energy efficient hybrid architecture for high resolution that pipelines two SAR ADCs, coupled by a residue amplifier, as shown in Fig. 1. The two SAR ADCs work as high-resolution sub-ADCs for the two pipeline stages to give the SAR-assisted pipeline ADC several advantages over conventional flash sub-ADC based pipeline ADCs and conventional SAR ADCs [2]. We improve ADC linearity and reduce amplifier power consumption in a pipeline ADC as we increase the resolution of the first-stage sub-ADC [3]. A SAR sub-ADC uses less power than a flash sub-ADC. Another important benefit of the SAR first-stage sub-ADC is that it removes sampling mismatch between the sub-ADC and the MDAC, thereby removing the need for a dedicated frontend SHA. The SAR-assisted pipeline architecture also has benefits over the conventional SAR architecture.

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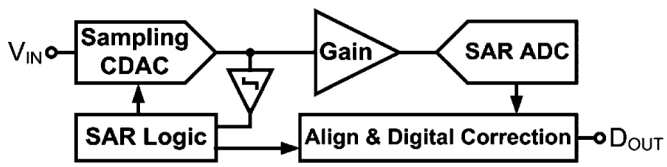

Fig. 1. SAR-assisted pipeline ADC block diagram.

The SAR ADCs in a SAR-assisted pipeline ADC have a much lower resolution than the overall ADC resolution, greatly relaxing the required comparator noise performance. In addition, pipelining relaxes the speed bottleneck of the conventional SAR architecture. The SAR-assisted pipeline ADC tolerates settling errors of the first-stage SAR capacitive DAC (CDAC) as long as these remain within the error correction range of the stage redundancy. Therefore, we can increase the speed of the first stage SAR ADC compared to the conventional SAR ADCs.

Despite these benefits, the use of a double-cascoded telescopic OTA based switched-capacitor (SC) residue amplifier in conventional SAR-assisted pipeline ADCs [1], [2], [4] limits efficiency because the OTA is power hungry and has a limited output swing. The limited output swing necessitates a reduced residue gain and requires power consuming second-stage reference scaling [1], [2], or the use of an R-2R DAC based second-stage SAR ADC [4]. Dynamic amplifiers, which operate as open-loop time-domain integrators, are a lower power alternative for residue amplification [5]–[11]. Although integration provides the benefit of noise-filtering [8], [9], the open-loop nature of dynamic amplification requires calibration to achieve accurate residue gain, and the calibration increases design complexity and test cost, and limits the robustness to process, supply voltage, and temperature (PVT) variation [6].

This paper introduces a 13 bit 50 MS/s fully-differential ring amplifier based SAR-assisted pipeline ADC [12], which achieves better efficiency (6.9 fJ/conversion·step) than conventional approaches and does not need calibration. A comparison of the Walden FOM (fJ/conversion·step) for conventional approaches (Fig. 2) shows that calibrated SAR-assisted pipeline ADCs with dynamic amplifiers[1] tend to achieve better efficiency. Instead, this work presents a new fully differential ring amplifier that enables accurate SC residue amplifier gain without the need for calibration. This ring amplifier has the

[1][5]–[11] achieve higher speed by using a 2× interleaved architecture and advanced CMOS processes (40 nm or 28 nm).

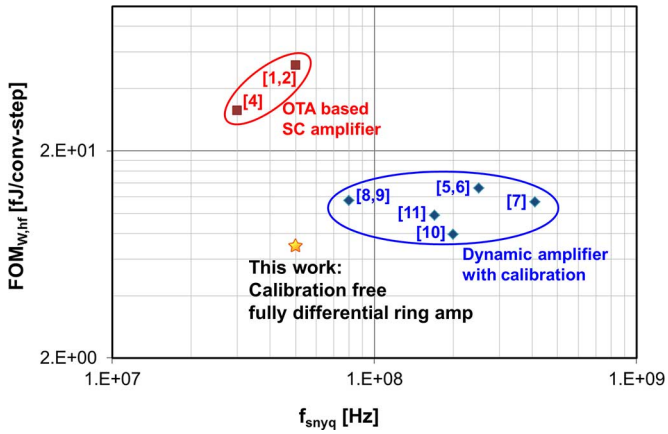

Fig. 2. Walden FOM comparison with conventional SAR-assisted pipeline ADCs.

advantages of energy efficient slew-based charging as well as a near rail-to-rail output swing, and is robust to PVT variation.

This work also improves the accuracy and the energy efficiency of the CDAC in the first-stage SAR sub-ADC. The first-stage CDAC draws a considerable amount of power from the references since it has a large capacitance to achieve low kT/C noise for high resolution. In addition, the accuracy of the first-stage CDAC must satisfy the linearity requirements of the full ADC resolution because DAC errors are not corrected by digital error correction. [8], [9] reduce the first-stage CDAC switching energy by floating three quarters of the two MSB capacitors and the remaining LSB capacitors during the three MSB decisions, but conventional approaches [5]–[11] still need to calibrate the first-stage CDAC in order to meet the required linearity. This paper presents an improved first-stage CDAC switching technique, which we name *floated detected-and-skip* (FDAS) switching, that further reduces the first-stage CDAC switching energy and also improves DAC linearity to achieve 13 bit linearity without calibration.

The remainder of this paper is organized as follows. Section II briefly reviews conventional single-ended ring amplifiers and introduces the new fully differential ring amplifier. Then, Section III presents the architecture of the prototype ADC, Section IV explains how FDAS first-stage CDAC switching reduces the CDAC switching energy and improves linearity, and Section V gives a detailed description of the ADC implementation. Finally, in Section VI, we present measurements of the prototype ADC, and conclude the paper in Section VII.

II. Fully-Differential Ring Amplifier

In this section, we briefly review conventional single-ended ring amplifiers and discuss their benefits and drawbacks. Then, we introduce the fully differential ring amplifier and give a detailed explanation of its operation.

A. Single-Ended Ring Amplifiers Review

The ring amplifier [13], Fig. 3(a) is an energy-efficient wide-swing alternative to an OTA for SC circuits. A ring amplifier is essentially a first-stage offset canceled three-stage inverter amplifier that is stabilized in a feedback network by operating the last stage in the subthreshold region when the amplifier input (V_{IN}) approaches desired common-mode voltage. The last stage is biased in the subthreshold region by using a split second stage and by applying floating offset voltages to the inputs of the two second stages. These floating offset voltages are applied using capacitors C_2 and C_3, switches, and an external offset voltage, V_{OS}. Subthreshold operation of the last stage ensures a high output resistance to form a dominant pole for stable feedback operation. Ring amplifiers have several important advantages over OTAs [13], [14]. First, they easily produce high gain from the three cascaded gain stages. Second, ring amplifiers achieve efficient slew-based charging, as the last stage operates as digital switch during slewing and is in cut-off (in deep subthreshold) when the amplifier is settled. Third, ring amplifiers have an almost rail-to-rail output swing because the last stage is a simple inverter operating in subthreshold region.

We earlier introduced a single-ended self-biased ring amplifier [14], Fig. 3(b), which improves robustness to PVT variation and is more practical and power efficient than the original ring amplifier. The use of high threshold voltage devices in the last stage extends the stable offset voltage range since high threshold voltage devices offer orders-of-magnitude higher output resistance for a given gate-source voltage. The resistor, R_B, applies an offset voltage to the gates of last stage transistors as shown in Fig. 3(b). The IR drop caused by the short circuit current of the second-stage inverter flowing through R_B dynamically applies an offset voltage to the last stage gates when V_{IN} is close to desired common mode voltage. With this resistor, the gates of the last stage are still driven to rail-to-rail when V_{IN} is away from the common mode voltage, ensuring maximum slew. This dynamic offset formed by the resistor gives us two benefits over the ring amplifier in [13]. First, we can auto-zero the combined three stages for improved PVT tolerance, since the ring amplifier now looks like a simple cascade of three inverter stages, without switches and external biases. Another benefit of the resistor-based dynamic offset is that it reduces the power consumption of the first inverter for a given first-stage bandwidth,[2] because it decreases the loading on the first-stage inverter by reducing the number of second-stage elements.

Existing ring amplifiers are single-ended and therefore these ring amplifiers have all of the disadvantages of single-ended structures. These disadvantages include the lack of inherent common mode and supply rejection, and the susceptibility to even order harmonics. The use of pseudo-differential structures and pseudo-differential common mode feedback (CMFB) [13], [14] (Fig. 4) can somewhat alleviate these problems. The pseudo-differential CMFB in Fig. 4 consists of the capacitors C_{S+}, C_{S-} and C_F, related switches, and the common mode voltage reference (V_{CM}). C_{S+} and C_{S-} sense the deviation of the output common mode from V_{CM} and feedback this to the ring amplifier inputs using C_F. However, this pseudo differential CMFB also reduces the effective ring amplifier gain to

[2]For a power constraint ring amplifier design, both the required transconductance of the first stage for noise, and the required bandwidth of the first stage for stability determine the power consumption of the first stage.

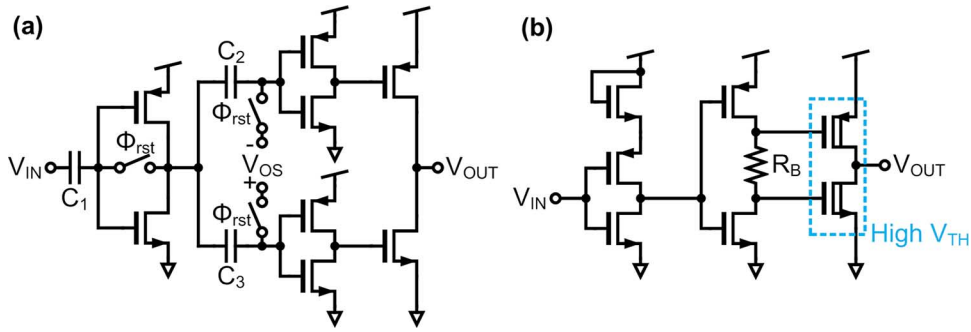

Fig. 3. Conventional ring amplifiers. (a) Original ring amplifier [13]; (b) self-biased ring amplifier [14].

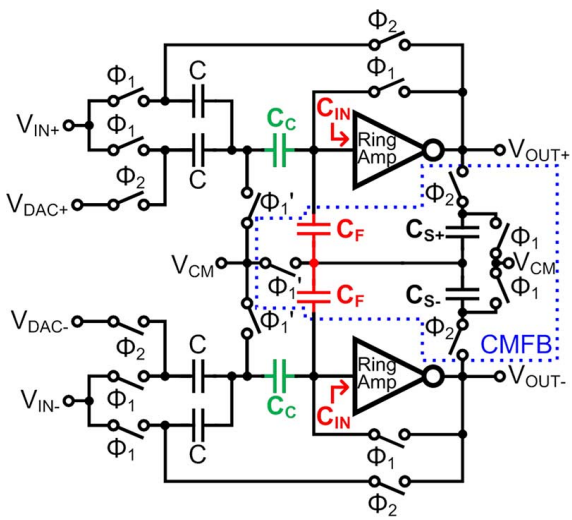

Fig. 4. Pseudo-differential MDAC gain stage in [14].

$A_V \cdot C_C/(C_C + C_F + C_{IN})$ due to the capacitive divider formed at the input of the ring amplifier, where A_V is the small signal gain of the ring amplifier, C_C is the offset canceling capacitance for auto-zero, and C_{IN} is the input parasitic capacitance of the ring amplifier.

B. Fully Differential Ring Amplifier

We introduce a new fully differential ring amplifier [12] that fully utilizes the ring amplifier gain and solves the limitations of the single-ended structure. A single differential ring amplifier replaces the two single-ended ring amplifiers in the conventional pseudo differential implementation. Fig. 5 shows the fully differential ring amplifier along with the bias and CMFB circuits. In order to make the ring amplifier fully differential, we replace the first stages of the two self-biased ring amplifiers [14] with a single differential pair. We use the current reuse technique to reduce the thermal noise of the first stage, which is the dominant noise source in the ring amplifier. In order to reduce the thermal noise, we increase the transconductance of the first stage since thermal noise is inversely proportional to transconductance. The use of both PMOS and NMOS input devices maximizes transconductance for a given current bias. To save power, an enable switch at the bottom of the NMOS tail current source, controlled by signal Φ_{EN}, turns off the ring amplifier when it is not used.

The first stage has both PMOS and NMOS tail current sources, which means that the first stage functions as a current starved inverter for the common mode of the input. A PMOS triode device based CMFB [15], consisting of M_4, M_5, and M_6, coarsely sets the common mode at the output of the first stage during auto-zero. The widths of the transistors in the bias circuit are 8 times smaller than the widths of the corresponding transistors in the half circuit of the first stage. V_{CM} is used as the cascode bias voltage for the bias circuit on the left hand side of Fig. 5 replicating the input voltage to the first-stage PMOS and NMOS devices. The use of V_{CM} as the cascode bias voltage also sets the ring amplifier input close to V_{CM}. The first stage (and also the ring amplifier) produces the highest gain when the inputs, V_{IN+} and V_{IN-}, are close to V_{CM}. Since the auto-zero sets the ring amplifier input and output voltage close to the input voltage which produces the highest gain, which is around V_{CM} in this case, the bias circuit sets the input voltages of the ring amplifier close to V_{CM} during auto-zero. We also use a separate SC CMFB circuit to set the overall output common mode of the ring amplifier to V_{CM} during the amplification phase. We do not perform CMFB on the ring amplifier output during auto-zero because the ring amplifier output common mode does not affect the ring amplifier differential input offset.

The second and third stages are inverter-like structures. As with the self-biased ring amplifier [14], the resistors, R_B, (Fig. 5) in the second stages dynamically apply offset voltages to the last stages. A limitation is that this dynamic biasing reduces the $|V_{DS}|$ of the second-stage transistors when current is flowing. In steady state, this causes the second-stage transistors to operate close to (or in) the triode region, greatly reducing the second-stage gain and also the gain of the entire ring amplifier. We use high V_{TH} devices in the second stage to prevent this gain reduction. The higher threshold voltage extends the second-stage output voltage range for which the transistors operate in saturation. The simulated small-signal ring amplifier gain is higher than 80 dB for an output swing from 0.1 V to 1.1 V with a 1.2 V supply.

III. Proposed ADC Architecture

The prototype ADC [12] consists of a 6 bit first-stage SAR ADC, a 32× residue gain stage based on the fully differential ring amplifier, and an 8 bit second-stage SAR ADC. Fig. 6 shows the proposed ADC architecture. The ADC resolves 13 bit after digital correction with a single bit of stage

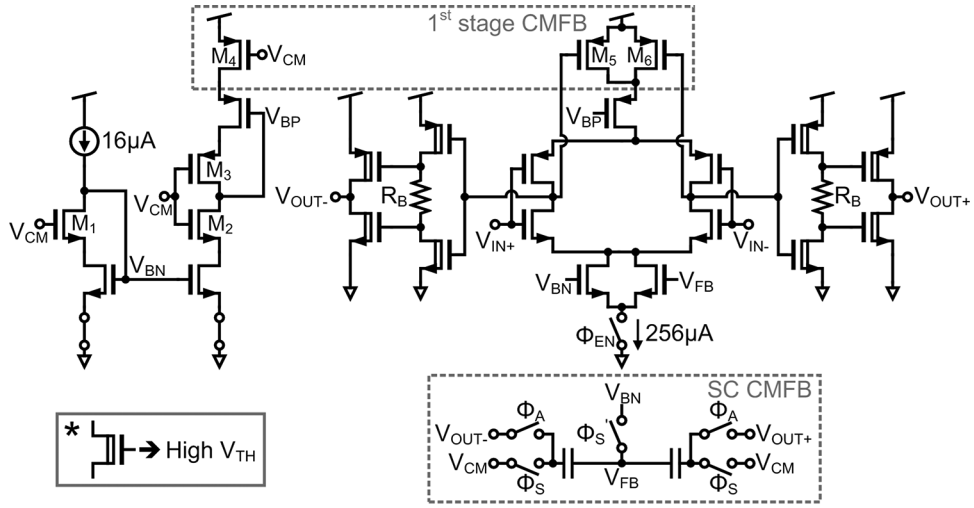

Fig. 5. Fully differential ring amplifier, bias, and CMFB.

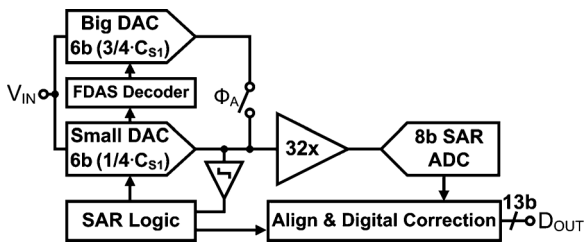

Fig. 6. Proposed ADC architecture.

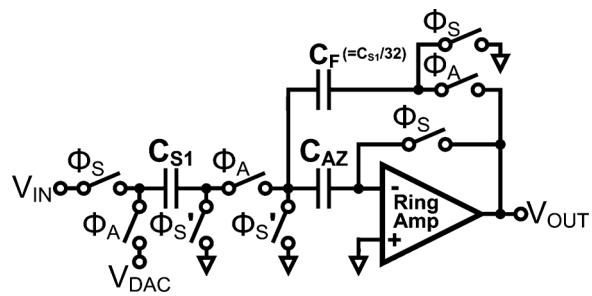

Fig. 7. Residue gain stage structure. Actual implementation is fully differential.

redundancy. The ADC accepts a 2.4 $V_{pk-pk\ diff}$ rail-to-rail input. Unlike conventional SAR-assisted pipeline ADCs [1], [2], [4]–[11], this work uses a full residue gain of 32, considering a single bit of stage redundancy, thanks to the wide output swing of the ring amplifier—this makes the second stage simpler and more efficient, and further relaxes the second-stage noise requirement. With the full residue gain and one bit of redundancy the ideal output range of the residue gain stage is from 0.3 V to 0.9 V, assuming the first-stage CDAC and comparator are ideal. The rest of the ring amplifier output range accommodates the 1 bit redundancy.

The first-stage SAR CDAC, as shown in Fig. 6, is divided into two separate capacitor arrays, *Big DAC* and *Small DAC*, to reduce the first-stage CDAC switching energy[3] and the INL due to the first-stage CDAC capacitor mismatch. The total sampling capacitance (differential) of the first-stage CDAC is 4 pF to meet the 13 bit kT/C noise requirement for residue generation. On the other hand, the first-stage SAR sub-ADC needs only to achieve 6 bit kT/C noise performance. In order to utilize these differing noise requirements to both reduce the CDAC switching energy and to improve linearity, we divide the first-stage CDAC into two CDACs, as shown in Fig. 6. The SAR ADC uses only *Small DAC*, which has a quarter of the sampling capacitance, to reduce power consumption. The remaining three quarters of the sampling capacitance is contained in *Big DAC*. Merged capacitor switching (MCS) [17] in the SAR ADC reduces the SAR DAC energy consumption. In addition, bottom plate input sampling enhances the accuracy of the MCS based SAR ADC by setting the comparator input to the common mode voltage during sampling, thus avoiding the effects of the nonlinear parasitic capacitance on the comparator input. Asynchronous SAR logic [18] eliminates the need for a high frequency clock and reduces errors due to comparator meta-stability.

Big DAC samples the same input signal as *Small DAC*, and together with *Small DAC* generates a residue voltage based on the decisions from the *Small DAC* based SAR ADC. Energy-efficient switching is achieved with the FDAS CDAC switching technique, which is derived from [19]. (Details of how FDAS switching reduces the CDAC switching energy and improves linearity of the first-stage CDAC are discussed in the next section.) When the first-stage conversion is finished, the residues of *Big* and *Small DACs* are merged together to meet the 13 bit kT/C noise requirement and are then amplified by $32\times$ using the residue amplifier. Mismatch between the overall DAC and the quantized value of the *Small DAC* SAR ADC is corrected by the 1 bit stage redundancy.

As shown in Fig. 7, we use an auto-zeroed fully-differential ring amplifier based SC amplifier for residue amplification. Φ_A controls the amplification phase, and Φ_S and Φ'_S are sampling/auto-zero phase control signals. The actual implementation is fully differential. Auto-zeroing is used to fully utilize the output swing of the ring amplifier so that we can maximize the digital correction range. A large (4 pF) offset cancelation capacitor,

[3]A similar technique, independently developed in [16], divides the first-stage CDAC to reduce the first-stage CDAC switching energy.

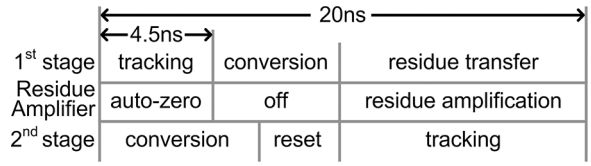

Fig. 8. Simplified ADC timing diagram.

C_{AZ}, reduces auto-zero noise folding [20]. However, the use of a big C_{AZ} capacitance does not increase power consumption, because the sampled voltage on C_{AZ} stays constant. This big capacitance also stabilizes the ring amplifier during the auto-zero phase by presenting a large load to the ring amplifier output, and reducing the dominant pole frequency and the slew rate. The small feedback factor ($\sim 1/33$) during the amplification phase also helps the stabilization of the ring amplifier [13].

As shown in the simplified ADC timing diagram, Fig. 8, the ring amplifier is turned off during the first-stage SAR ADC conversion to reduce the power consumption. The amplification starts asynchronously after the first-stage SAR ADC conversion is complete to maximize the duration of the residue amplification phase. The amplified residue is sampled and then quantized by an 8 bit second-stage SAR ADC, which also uses MCS, bottom plate input sampling, and asynchronous SAR logic. As shown in Fig. 8, the second-stage CDAC is reset after the 8 bit decision so that residue amplification always starts from V_{CM}. This reset operation improves the power efficiency of the ring amplifiers by halving the maximum slew rate required of the ring amplifier [14].

IV. FDAS First-Stage CDAC Switching

As mentioned in the previous section, we use FDAS switching in the first-stage CDAC. This section explains the operation of FDAS switching, and how it both reduces the first-stage CDAC switching energy and improves the DAC linearity.

A. Switching Energy Reduction

One of the switching energy losses in conventional SAR operation comes from the binary search. Fig. 9 shows an example of residue generation for a 4 bit *Big DAC* using MCS switching. In this example, *Big DAC* is switched directly based on the *Small DAC* MCS decisions. The DAC output voltage, V_{DAC}, starts at the inverse of the DAC input ($-V_{IN}$) because we use bottom plate input sampling. As shown in Fig. 9, if we generate the *Big DAC* residue using a binary search and MCS, we will have opposite direction switching in some cases. Although this opposite direction switching is necessary for the binary search, it is wasteful for residue generation. However, we can avoid this wasteful switching energy since we already know the decisions of the *Small DAC* SAR ADC.

In order to reduce this switching energy loss for *Big DAC*, we adopt detect-and-skip (DAS) switching [19]. Fig. 10 shows an example of DAS switching for residue generation in a 4 bit *Big DAC*. DAS detects the opposite direction switching from the *Small DAC* SAR ADC decisions, and skips this opposite direction switching for *Big DAC* by connecting the corresponding switches to V_{CM}. Even though we avoid opposite direction switching using DAS switching, we still get the same

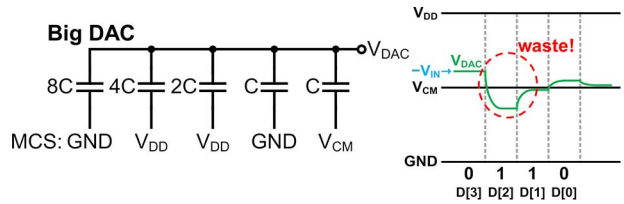

Fig. 9. MCS switching 4 bit *Big DAC* residue generation example. The bottom plates are switched to the final states.

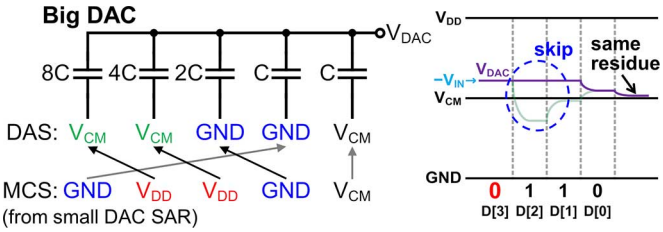

Fig. 10. Detect-and-skip (DAS) switching 4 bit *Big DAC* residue generation example when the MSB (D [3]) of *Small DAC* SAR is 0. The bottom plates are switched to the final states.

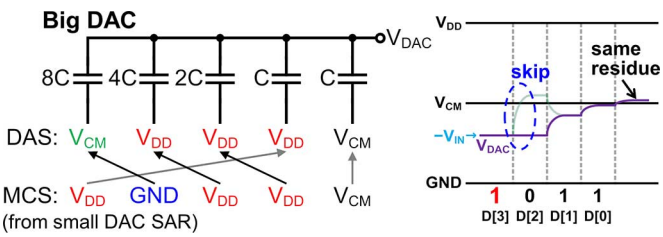

Fig. 11. Detect-and-skip (DAS) switching 4 bit *Big DAC* residue generation example when the MSB (D [3]) of *Small DAC* SAR is 1. The bottom plates are switched to the final states.

overall residue as with MCS switching. Although it might be expected that decoding the *Small DAC* SAR decisions for DAS switching would require a complicated algorithm [19], it turns out that a simple decoding method can be used. As shown in Fig. 10, when the MSB of the *Small DAC* SAR decision is 0, this decoding is a simple left circular shift of the *Small DAC* SAR decision results and the replacement of V_{DD} connections with V_{CM} connections. Similarly, as shown in Fig. 11, when the MSB of the *Small DAC* SAR decision is 1, the decoding is a simple left circular shift of the *Small DAC* SAR decision results and the replacement of ground (GND) connections with V_{CM} connections. In this way, we avoid significant switching energy loss related to the binary search in the first-stage CDAC.

Another switching energy loss in the conventional SAR CDAC operation comes from the successive capacitor switching needed after each decision. A conventional SAR CDAC successively switches a capacitor after every decision in the binary search. Fig. 12(a) shows an example of successive switching in a 2 bit CDAC. When the MSB switch flips from ground to reference voltage, V_R, the CDAC consumes CV_R^2 of switching energy, and then when the LSB switch flips, the CDAC consumes a further $0.25CV_R^2$ of switching energy. Therefore, in this example, the CDAC consumes a total switching energy of $1.25CV_R^2$. Although this energy consumption due to successive switching is unavoidable with a single capacitor array SAR DAC, here since we already know

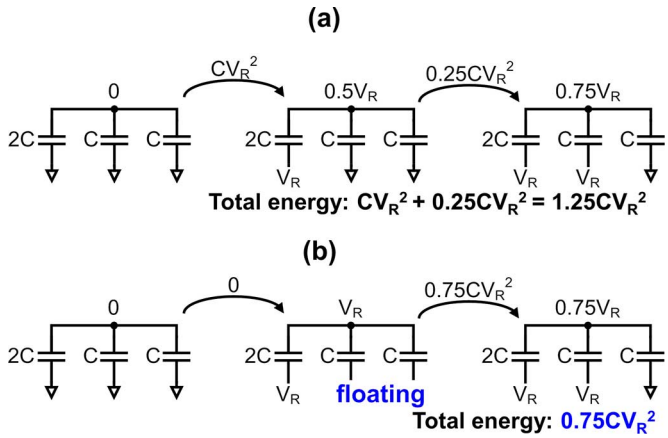

Fig. 12. Two bit CDAC switching example. (a) Successive switching; (b) floated detect-and-skip switching.

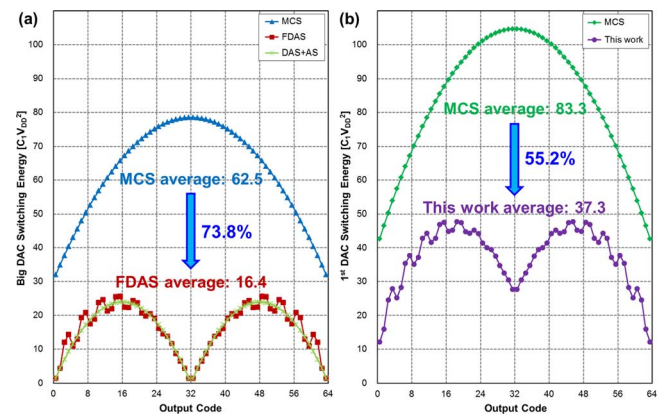

Fig. 13. Calculated 6 bit CDAC switching energy comparison. (a) *Big DAC* switching energy. (b) The first-stage CDAC switching energy. *Big DAC* use $3C_1$ as a unit capacitor and the first-stage CDAC use $4C_1$ as a unit capacitor. The CDACs uses V_{DD} and ground as references.

the result from the *Small DAC* SAR ADC we can avoid some of this switching energy for *Big DAC*.

In order to reduce switching energy loss from successive switching, [19] uses aligned switching (AS) together with DAS. This technique sets *Big DAC* switches only after the *Small DAC* SAR ADC is completely finished. However, aligned switching requires additional settling time or alternatively bigger switches with increased DAC encoder power consumption to minimize the additional settling time. Instead of using DAS and AS together, we introduce floated DAS (FDAS) in which we flip *Big DAC* switches immediately after each corresponding *Small DAC* SAR bit decision, while the undecided capacitors are floated. Fig. 12(b) shows a 2 bit example of FDAS switching. When the MSB capacitor switch flips, the CDAC does not consume switching energy since there is no charge movement because all the other capacitors are floated. Then, when the LSB and the dummy switch flip, the CDAC consumes $0.75CV_R^2$ of switching energy. Thus, in this example we save $0.5CV_R^2$ of switching energy by using FDAS switching. Another benefit of FDAS switching is it does not require additional settling time for *Big DAC* switching. The MSB capacitors of *Big DAC* have plenty of settling time because MSB switching occurs early.

Fig. 13 shows comparisons of calculated 6 bit CDAC switching energy. When we compare FDAS *Big DAC* switching

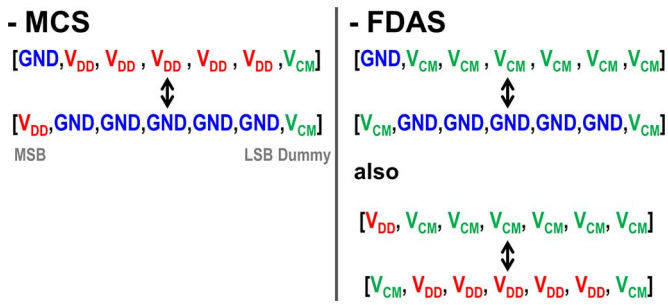

Fig. 14. Worst case INL of 6 bit CDAC switching for MCS and FDAS.

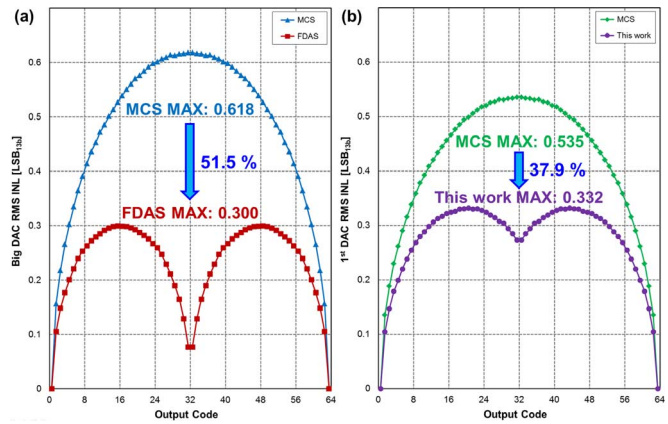

Fig. 15. Simulated RMS INL due to the first-stage CDAC mismatch with 10k iteration and a one sigma C_1 mismatch of 0.3 %. (a) RMS INL due to *Big DAC*, (b) RMS INL due to the first-stage CDAC. *Big DAC* use $3C_1$ as a unit capacitor and the first-stage CDAC use $4C_1$ as a unit capacitor.

with MCS *Big DAC* switching (Fig. 13(a)), FDAS consumes 74% less switching energy on average. FDAS *Big DAC* switching consumes slightly more switching energy (2.7%) than DAS with AS [19] [Fig. 13(a)] because the last two LSBs and the dummy switches flip together at the end of the *Small DAC* SAR decision. However, FDAS switching has the significant advantage of not requiring additional settling time for *Big DAC* and this allows us to reduce the size of *Big DAC* switches, which itself reduces the power consumption of the FDAS encoder. When we compare the first-stage DAC switching energy in this work (i.e., MCS *Small DAC* switching and FDAS *Big DAC* switching) with MCS only first-stage CDAC switching [Fig. 13(b)], this work consumes 55% less switching energy on average.

B. Linearity Improvement

FDAS (and also DAS, although not mentioned in [19]) switching also reduces INL errors due to the first-stage CDAC capacitor mismatch. As shown in Fig. 14, the worst case INL with MCS occurs when the MSB switch flips between V_{DD} and GND. However, the worst case INL with FDAS occurs when the MSB switch flips between GND and V_{CM}, or between V_{DD} and V_{CM}. Since the voltage swing is halved in FDAS switching, the worst case voltage error is also halved and thus the worst case INL is halved. This INL improvement is the same as for the early reset merged capacitor switching (EMCS) algorithm in [21]. In fact, FDAS decoding result is the same as EMCS algorithm decoding result. Fig. 15 shows the results

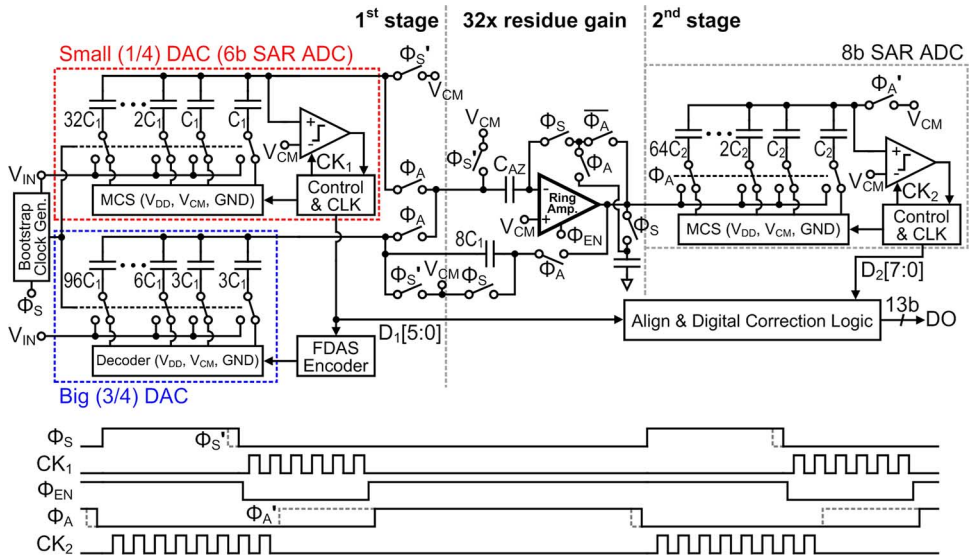

Fig. 16. Block diagram and timing of the prototype ADC (Actual implementation is fully differential). CK_1, CK_2, and rising edges of Φ_{EN}, Φ_A and Φ'_A are asynchronously generated.

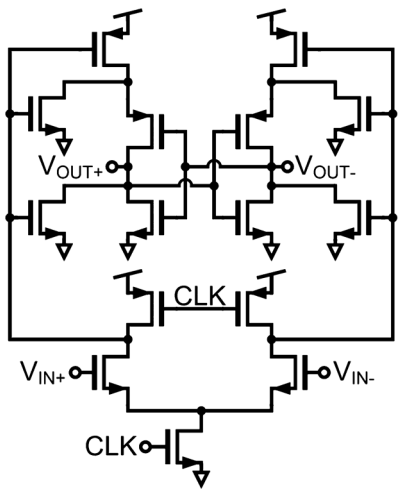

Fig. 17. Low noise single phase dynamic latched comparator [23].

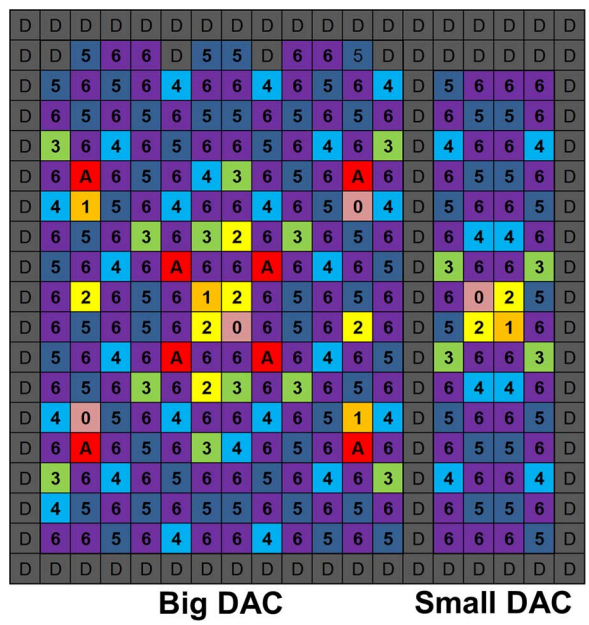

Fig. 18. Common centroid first-stage CDAC layout map. The letter A stands for the feedback capacitors for amplification, D stands for process dummies, 0 stands for the LSB dummies, and the rest of numbers stand for the corresponding bits in 6 bit DAC.

for Monte Carlo simulation of the RMS INL of the first-stage CDAC (10 k iterations) for a one sigma unit capacitor mismatch of 0.3%. The simulation shows that the maximum RMS INL for FDAS *Big DAC* switching is 52% lower than for MCS *Big DAC* switching [Fig. 15(a)]. The RMS INL due to the overall first-stage CDAC is 38% less than for an MCS only first-stage CDAC [Fig. 15(b)].

V. Detailed ADC Implementation

A 50 MS/s 13 bit SAR-assisted pipeline ADC [12] is implemented to demonstrate the effectiveness of the fully differential ring amplifier and FDAS first-stage CDAC switching. Fig. 16 shows a detailed ADC block diagram and the timing for the prototype ADC. We implement a bootstrap clock generator [22] which distributes the sampling clock and deep N-well bias voltages to the input switches of the first-stage CDAC. The improved auto-zero switching in [14] is used to eliminate the gain error caused by the parasitic capacitance across the auto-zero switch. The auto-zero capacitors, C_{AZ}, are implemented MIM capacitors to reduce bottom plate parasitic capacitance. The comparator (Fig. 17) used in this ADC is a low noise single-phase dynamic latched comparator [23]. The one sigma offset of the first-stage comparator is designed to be lower than 0.1 LSB at 6 bit resolution to ensure that the first-stage offset error stays within the one bit digital correction range. The SAR DACs are implemented with custom designed encapsulated MOM capacitors, laid out in common centroid as shown in Fig. 18. The unit capacitance of the first-stage CDAC, C_1, is 7.9 fF and the unit capacitance of the second-stage CDAC, C_2, is 2.6 fF.

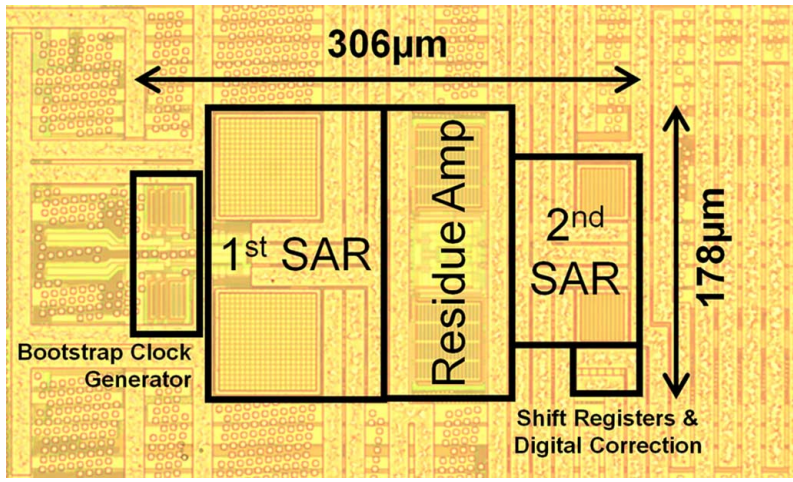

Fig. 19. Die microphotograph of prototype ADC.

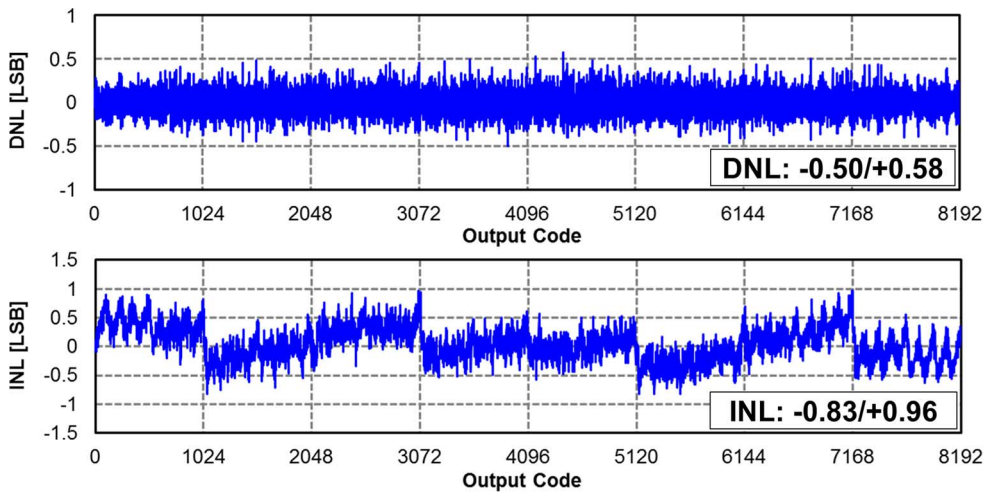

Fig. 20. Measured DNL and INL at 50 MSPS (Decimated by 2).

The ADC only requires a single reference voltage, V_{CM}, since it uses a full residue gain $(32\times)$, and both of the SAR ADCs support a rail-to-rail input. The SAR ADCs use V_{DD} and GND as the high and low references. The high reference is separated from the main V_{DD} in the chip and connected to the main V_{DD} on the test board for measurement purposes. The ADC requires a 25% duty cycle 50 MHz external clock for sampling. All the other control signals are generated on chip.

VI. Measurement Results

The prototype ADC is fabricated in a single-poly nine metal (1P9M) 1.2 V 65 nm CMOS process. The ADC occupies a small area of 0.054 mm^2, as shown in the die microphotograph in Fig. 19. A summary of the measured performance is given in Table I. The ADC output is decimated by two to avoid the effects of I/O switching noise on ADC performance. The ADC supports a full-scale rail-to-rail swing differential input signal of 2.4 V_{pk-pk}. The ADC achieves 13 bit linearity without calibration, thanks to the linearity improvement due to FDAS CDAC switching. Linearity plots (Fig. 20) measured at 13 bit and at a full conversion rate of 50 MS/s, show that the measured DNL and INL are within $-0.50/+0.58$ LSB and $-0.83/+0.96$ LSB, respectively. As shown in the measured spectrums (Fig. 21), at a 50 MS/s the ADC achieves 71.5 dB SNDR (11.6 bit ENOB), 71.9 dB SNR, and 87.0 dB SFDR with a 10.1 MHz input, and 70.9 dB SNDR (11.5 bit ENOB), 71.3 dB SNDR, and 84.6 dB SFDR with a Nyquist frequency input. Fig. 22 summarizes the measured SFDR, SNR, and SNDR versus input frequency. The ADC has a quite flat SNDR response and higher than 83.9 dB SFDR for all input frequencies. The ADC has linear SNDR response up to the full-scale (Fig. 23).

We swept the ring amplifier power supply voltage to check the robustness of the fully differential ring amplifier. For a rail-to-rail input swing and a Nyquist frequency input, the SFDR and SNDR remain flat over a ring amplifier power supply voltage range from 1.15 V to 1.25 V (Fig. 24), deviating by 0.73 dB and 0.45 dB, respectively. This proves that the fully differential ring amplifier is very robust to supply voltage variation. The fully differential ring amplifier has a flat gain response over supply voltage variation. The second-stage gain decreases when the supply voltage increases since the higher IR drop from the dynamic offset biasing resistor pushes the second-stage transistors towards the triode region. On the other hand, the higher offset

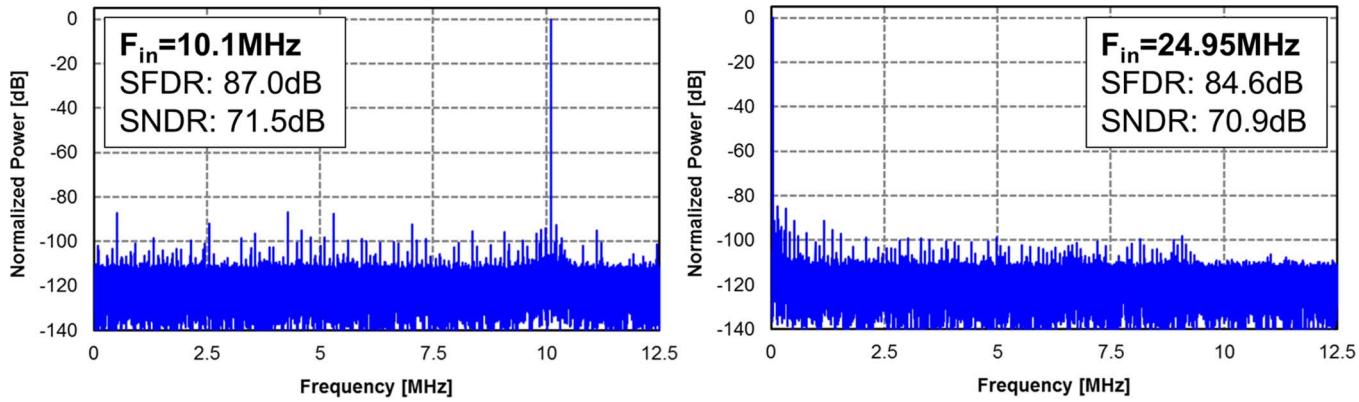

Fig. 21. Measured spectrums for 10.1 MHz and 24.95 MHz inputs sampled at 50 MS/s (Decimated by 2, 65536 point FFT).

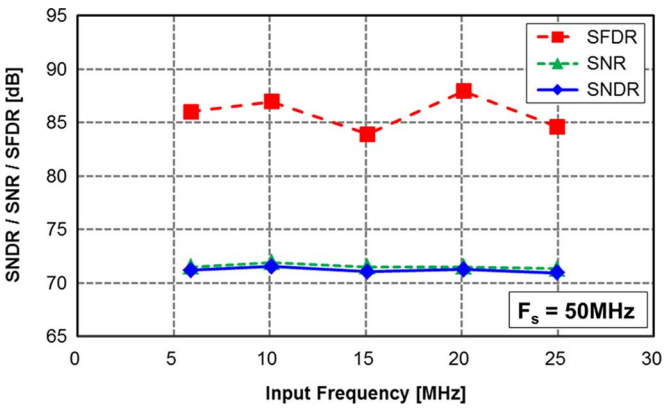

Fig. 22. Measured SFDR, SNR, and SNDR versus input frequency (Decimated by 2).

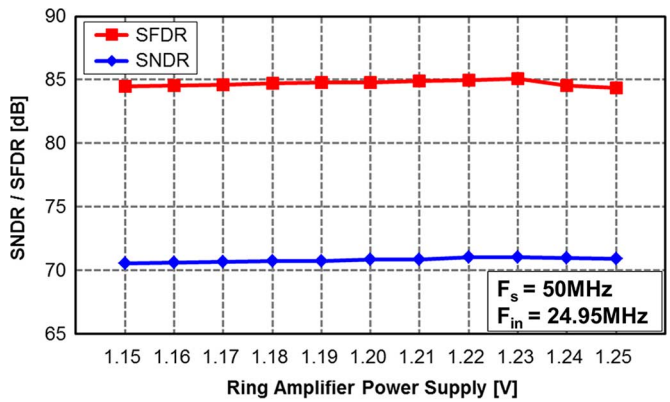

Fig. 24. Measured SNDR and SFDR versus ring amplifier power supply (Decimated by 2).

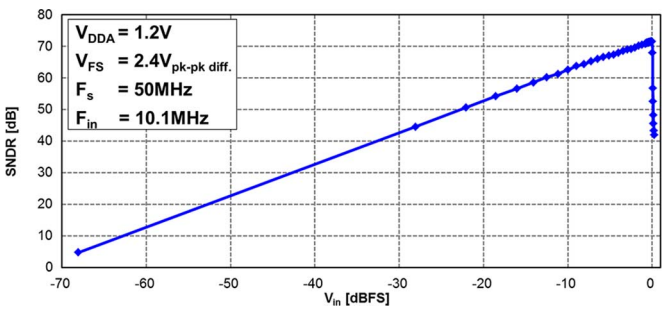

Fig. 23. Measured SNDR versus input amplitude (Decimated by 2).

voltage due to the increased IR drop leads the last stage operating deeper in the subthreshold region resulting in a higher last stage gain. The gain changes in the second and the last stage are somewhat compensated; therefore the overall ring amplifier gain stays quite flat over a wide supply voltage range. Simulations indicate that the small signal gain of the fully differential ring amplifier decreases by only around 1 dB over a supply voltage range from 1.15 V to 1.25 V. We also swept the ambient temperature to check the robustness of the fully differential ring amplifier. The ADC has a higher than 81.0 dB measured SFDR and a higher than 69.7 dB measured SNDR over a $-20°C$ to $80°C$ temperature range (Fig. 25), proving that the fully differential ring amplifier is also quite robust to temperature variation.

TABLE I
ADC PERFORMANCE SUMMARY

Resolution	13 bits	
Supply	1.2 V (Ring amp, SAR logic, V_{REF+}), 0.6 V (V_{CM}), 0.8 V (Shift register & digital correction)	
Sampling Rate	50 MS/s	
Technology	65 nm 1P9M CMOS	
Active Area	0.054 mm^2	
Input Range	2.4 V_{pk-pk} differential	
DNL	+0.58/-0.50 LSB	
INL	+0.96/-0.83 LSB	
Power Consumption	1 mW Total: 366 µW (Ring amp), 510 µW (SAR logic, bootstrapping clock), 95 µW (Ref.), 29 µW (Shift reg. & correction)	
	F_{in}=10.1 MHz	**F_{in}=24.95 MHz**
SNDR	71.5 dB	70.9 dB
SNR	71.9 dB	71.3 dB
SFDR	87.0 dB	84.6 dB
ENOB	11.6 bits	11.5 bits
FoM_W [P/($F_s \cdot 2^{ENOB}$)]	6.5 fJ/conv-step	6.9 fJ/conv-step
FoM_S [SNDR+10log(F_s/2/P)]	175.5 dB	174.9 dB

The ADC consumes a total power (excluding I/O) of 1 mW at the full conversion speed of 50 MS/s, with a Nyquist frequency input. This result is equivalent to Walden and the Schreier FoMs

TABLE II
PERFORMANCE COMPARISON WITH THE CONVENTIONAL SAR-ASSISTED PIPELINE ADC

		This Work	VLSI 2010 [1], [2]	ISSCC 2012 [4]	ISSCC 2014 [8]	VLSI 2014 [10]
Resolution [bits]		13	12	14	14	14
F_S [MS/s]		50	50	30	80 (2x interleaved)	200 (2x interleaved)
Technology		65 nm CMOS	65 nm CMOS	130 nm CMOS	28 nm CMOS	28 nm CMOS
Active Area [mm^2]		0.054	0.16	0.24	0.137	0.35
Analog Supply [V]		1.2	1.3	1.2	1.0	0.9
ADC FS [$V_{pk\text{-}pk\ diff.}$]		2.4	2	2	1.4	-
Residue Amp. Structure		Fully diff. ring amplifier	Telescopic amplifier	Telescopic amplifier	Dynamic amplifier	Dynamic amplifier
Calibration		No	No	No	Yes (gain, offset, DAC)	Yes (gain, offset, DAC)
|INL| [LSB]		≤ 0.96	≤ 1.5	≤ 3.52	-	-
|DNL| [LSB]		≤ 0.58	≤ 0.75	≤ 0.89	-	-
Nyquist freq.	SNDR [dB]	70.9	64.4	70.4	66.0	65.0
	SFDR [dB]	84.6	75.0	79.6	74.0	-
Total Power [mW]		1.0	3.5	2.54	1.5	2.3
Amp. Power [mW]		0.366	2.6	0.47	-	-
FOM_W [fJ/conv-step]		6.9	51.8	31.3	11.5	7.9
FOM_S [dB]		174.9	162.9	168.1	170.3	171.4

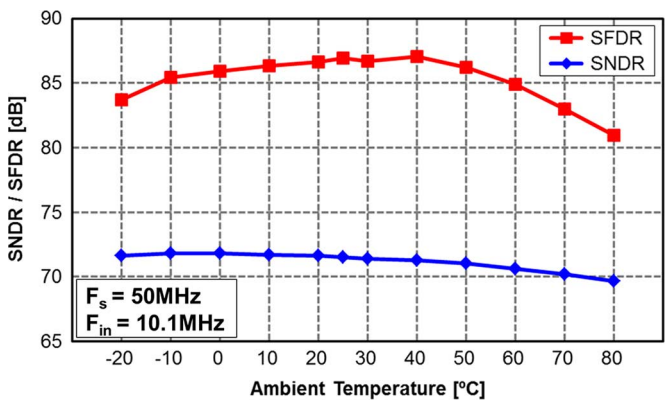

Fig. 25. Measured SNDR and SFDR versus ambient temperature (decimated by 2).

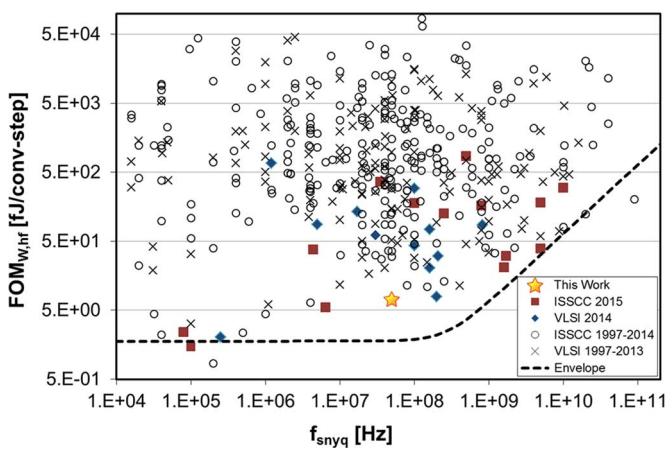

Fig. 26. Walden FOM comparison with ADCs presented at ISSCC 1997–2015 and VLSI 1997–2014 [24].

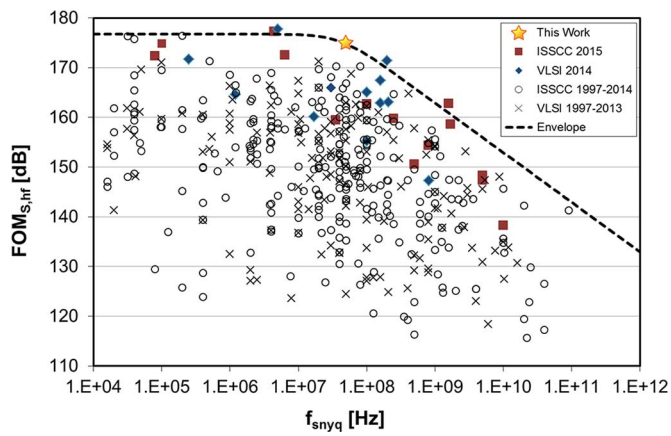

Fig. 27. Schreier FOM comparison with ADCs presented at ISSCC 1997–2015 and VLSI 1997–2014 [24].

of 6.5 fJ/conversion·step and 175.5 dB, respectively, for 10.1 MHz input, and 6.9 fJ/conversion·step and 174.9 dB, respectively, for a Nyquist frequency input. The total power consumption is comprised of 366 μW for the ring amplifier, 510 μW for the SAR logic, comparators, and the bootstrapping clock generator, 95 μW for the references, and 29 μW for the shift register and digital correction power.

Table II compares the performance of the prototype ADC with conventional SAR-assisted pipeline ADCs. This work achieves less than 1 LSB INL at 13 bit resolution, and the highest SNDR and SFDR without calibration. In addition, this work has the best Walden and Schreier FoMs. Figs. 26 and 27 compare the Walden and the Schreier FoMs with ADCs presented at ISSCC 1997–2015 and VLSI symposium 1997–2014 [24]. This work achieves state-of-the-art Walden and Schreier FoMs.

VII. Conclusion

This paper introduces a fully-differential ring amplifier based SAR-assisted pipeline ADC. The new fully-differential ring amplifier solves the limitations of conventional single-ended ring amplifiers, and allows us to achieve power efficient amplification without calibration, thanks to energy-efficient slew-based charging, an almost rail-to-rail output swing, and higher overall gain. We introduce FDAS first-stage CDAC switching, which reduces the CDAC switching energy and also improves DAC linearity, by utilizing the differing noise requirements of the first-stage sub-ADC and MDAC. With these two techniques, the calibration free prototype ADC achieves 70.9 dB SNDR for a Nyquist frequency input sampled at 50 MS/s and consumes only 1 mW. The Walden and the Schreier FoMs of this work are 6.9 fJ/conversion·step and 174.9 dB, respectively, which are the best reported to date for an ADC with a sampling speed faster than 6 MS/s.

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