A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC

Chun-Cheng Liu, *Member, IEEE*, Mu-Chen Huang, and Yu-Hsuan Tu

***Abstract*— This paper presents an energy-efficient successive approximation register (SAR)-assisted digital-slope analog-to-digital converter (ADC) architecture for high-resolution applications. The proposed hybrid ADC combines a low-noise fine digital-slope ADC with a low-power coarse SAR ADC. The coarse SAR ADC rapidly approximates the input signal and produces a small residue signal for the succeeding fine ADC. The fine digital-slope ADC linearly approaches the small residue signal. A prototype was fabricated in 1P8M 28 nm CMOS technology. At 100 MS/s, the ADC achieves a signal-to-noise-and-distortion ratio of 64.43 dB and a spurious free dynamic range of 75.42 dB at the Nyquist input frequency while consuming 0.35 mW from a 0.9 V supply. The resultant Walden and Schreier figures of merit are 2.6 fJ/conversion-step and 176.0 dB, respectively. The ADC occupies an active area of 66 μm × 71 μm.**

***Index Terms*— Analog-to-digital converter (ADC), digital-slope ADC, hybrid ADC, SAR ADC, SAR-assisted digital-slope ADC, successive approximation register (SAR).**

I. Introduction

THE successive approximation register (SAR) analog-to-digital converter (ADC) is a popular architecture for achieving high energy efficiency. The operation speed of SAR ADCs has improved with the scaling of CMOS technology. With growing transistor bandwidth, a single-channel SAR ADC can achieve a sampling speed of up to a few hundred MS/s with a resolution of 8 to 12 bits [1], [2]. Energy-efficient high-speed SAR ADCs are attractive for wireless communication systems, such as Wi-Fi and LTE. However, the signal-to-noise ratio (SNR) of high-speed SAR ADCs is mainly constrained by comparator noise and usually limited to below 60 dB. The tradeoff between the noise and power consumption of a comparator is not linear. The power consumption increases quadratically to suppress comparator noise in a limited comparison time [3]. Noise-tolerant SAR ADCs [4] reduce comparator power in the first few bit cycles by using a coarse comparator. However, the fine comparator in the remaining bit cycles still consumes significant power to achieve an SNR of greater than 60 dB. The data-driven noise-reduction technique [5] and the adaptive-tracking-averaging technique [6] enhance SNR by taking extra bit cycles to convert the least significant bits (LSBs). These techniques reduce comparator noise without a quadratic increase in power consumption. However, the additional bit cycles degrade the maximum operation speed of the ADCs.

SAR-assisted pipelined ADCs [7]–[12] achieve high SNR by pipelining two or more low-resolution SAR sub-ADC stages. The residue signal amplification between the sub-ADC stages relaxes the requirement for a low-noise comparator. In addition, splitting the ADC conversion into two or more low-resolution sub-ADCs increases conversion speed. However, a high-gain high-bandwidth amplifier is needed to avoid the gain error problem between stages, and design restrictions for advanced CMOS processes make high-performance amplifier design challenging. Using a dynamic [8]–[10] or low-gain amplifier [11] induces gain errors between stages and hence complicated background calibration is needed to overcome the process, supply voltage, and temperature (PVT) variations. The fully differential ring amplifier [12] achieves high gain and high bandwidth with high power efficiency, but the cascading first stage is not suited for operating with the low supply voltage in advanced CMOS processes. Moreover, the amplifier and the sampling capacitor in the back-end stages contribute extra noise and area to the ADC.

A dual-slope integrating ADC [13] transforms a voltage-domain signal into a time-domain signal using an integrator and a continuous-time comparator (CT-CMP). Then, the ADC quantizes the time-domain signal by a digital counter, which is triggered by a synchronous clock. The dual-slope ADC inherently has high linearity and low noise but its speed is low. The digital-slope ADC [14] replaces the integrator in the dual-slope ADC by an asynchronous switched capacitor (SC) operation while retaining the latter's low noise. It quantizes the time-domain signal using memory cells and an encoder instead of a digital counter. Hence, the digital-slope ADC achieves a much higher operation speed. However, the hardware grows exponentially with ADC resolution and the maximum conversion rate is halved with each extra bit of resolution. Therefore, the digital-slope ADC is unattractive for resolutions higher than 8 bits. To ameliorate this limitation, the present study proposes a hybrid ADC that combines a low-noise digital-slope ADC with a low-power SAR ADC to achieve high resolution without complicated hardware.

This work presents a 12-bit SAR-assisted digital-slope ADC [15] that combines a 6 bit fine digital-slope ADC with a 7 bit coarse SAR ADC. With a 0.9 V supply, the prototype achieves a 100 MS/s sampling rate and consumes only 0.35 mW. The ADC achieves a signal-to-noise-and-distortion ratio (SNDR) of 64.43 dB and a spurious free dynamic range (SFDR) of 75.42 dB at the Nyquist input frequency. The resultant Walden and Schreier figures of

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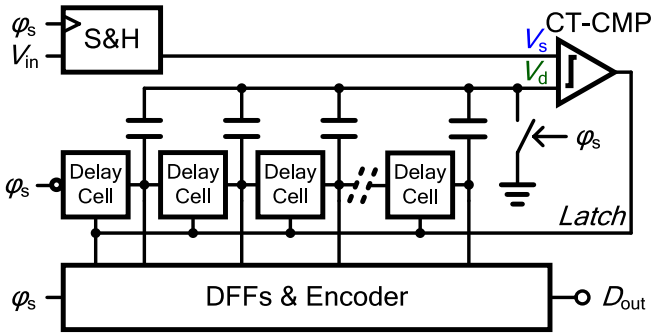

Fig. 1. Block diagram of an ansychronous digital-slope ADC.

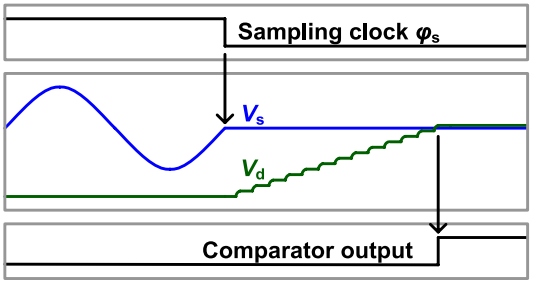

Fig. 2. Timing diagram of a digital-slope ADC.

merit (FoMs) are 2.6 fJ/conversion-step and 176.0 dB, respectively. These FoM values are the best reported to date for sampling rates higher than 10 MS/s. The ADC core fabricated in 1P8M 28 nm CMOS technology occupies an active area of only 66 μm $\times$ 71 μm.

The remainder of this paper is organized as follows. Section II introduces the architecture of the proposed ADC. Section III describes the detailed implementation of the proposed ADC and its key building blocks. Section IV shows the measurement results of the prototype ADC and a comparison to the state-of-the-art works. Finally, conclusions are given in Section V.

II. Proposed ADC Architecture

A. Review of Asynchronous Digital-Slope ADC

Fig. 1 shows a block diagram of an asynchronous digital-slope ADC [14]. The corresponding time diagram is sketched in Fig. 2. The asynchronous digital-slope ADC is composed of a sample-and-hold (S/H) circuit, a CT-CMP, delay cells, unit capacitors, D flip-flops (DFFs) and an encoder. The S/H circuit samples the input signal at the falling edge of sampling clock φ_s and holds the sampled signal V_s when the sampling clock signal is low. The voltage V_d is reset to ground during the sampling phase. After the input signal is sampled, V_d is switched up 1 LSB step by 1 LSB step at a constant interval controlled by the delay line. When the voltage V_d is higher than the sampled signal V_s, the output of the CT-CMP will change the output polarity and stop the delay propagation. To avoid some unnecessary switching in the encoder when delay propagating, the outputs of all delay cells are sampled by D flip-flops, which are all clocked with the *latch* signal. The sampled outputs represent a thermometer code that is proportional to the input signal. Finally, the encoder converts the thermometer code into binary to complete the conversion.

Similar to the SAR ADC architecture, the digital-slope ADC architecture is a simple and highly digital architecture. Both architectures achieve good power efficiency in advanced CMOS processes. However, there are some differences between them. The SAR ADC uses a binary search algorithm, whereas the digital-slope ADC uses a linear search algorithm. The SAR ADC needs at least N comparisons for an N-bit conversion, whereas the digital-slope ADC needs just one comparison [14]. For a SAR ADC conversion, the residue signal gets smaller with the SAR bit-cycling. A regenerative comparator makes comparison by sensing a very small static residue voltage in the LSB bit cycle. The input-output relation of a regenerative comparator is given by

$$V_{\text{out}} = V_{\text{in}} \cdot e^{T_c/\tau}. \tag{1}$$

The sense amplification of a smaller residue signal leads to a longer decision time to determine logical level "1" or "0". A metastable state occurs when the decision delay is longer than a limited comparison time, which is very critical in high-speed SAR ADCs.

For digital-slope ADC conversion, the CT-CMP measures signals by detecting a dynamic zero-crossing. The continuous ramping of the reference level prevents the CT-CMP from entering a metastable state and the output always flips with approximately a constant delay after the zero-crossing. The comparison time is given by

$$T_c = \frac{V_{\text{in}}}{V_{\text{LSB}}} \cdot \tau_u + T_{\text{latency}} \tag{2}$$

where τ_u is the latency of a delay cell and T_{latency} is the latency from the input zero-crossing to the output flipping. The comparison time T_c is linearly proportional to the input signal V_{in}. Hence, the digital-slope ADC is free of metastability regardless of the size of the input signal.

B. Proposed SAR-Assisted Digital-Slope ADC

The SAR ADC has good power efficiency for large-signal conversion, but suffers from comparator noise and metastability for small residue signals. The digital-slope ADC transforms a voltage-domain signal into a time-domain signal using digital ramping and a CT-CMP, and then performs quantization in the time domain. It inherits the low noise from the dual-slope ADC [13], so it achieves good noise suppression, but has limited resolution due to hardware complexity [14]. The present study proposes a hybrid ADC architecture that adopts a power-efficient SAR ADC for most significant bits (MSBs) conversion and a low-noise digital-slope ADC for LSBs conversion. The combination of a SAR ADC and a digital-slope ADC preserves their respective advantages and mitigates their limitations. Fig. 3 shows the block diagram of the proposed SAR-assisted digital-slope ADC. The coarse dynamic comparator (D-CMP) and SAR logic are used for the SAR coarse conversion. The fine CT-CMP, delay line, D-flip-flops, and encoder are used for the digital-slope fine conversion. The digital correction logic converts the output of the coarse

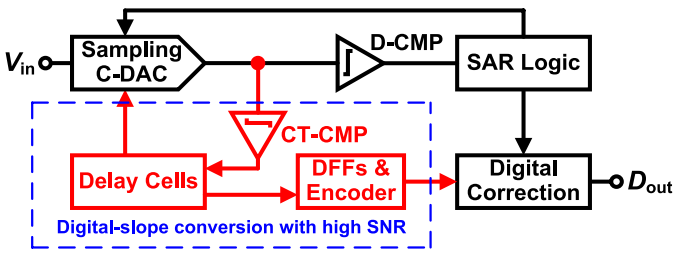

Fig. 3. Block diagram of the proposed SAR-assisted digital-slope ADC.

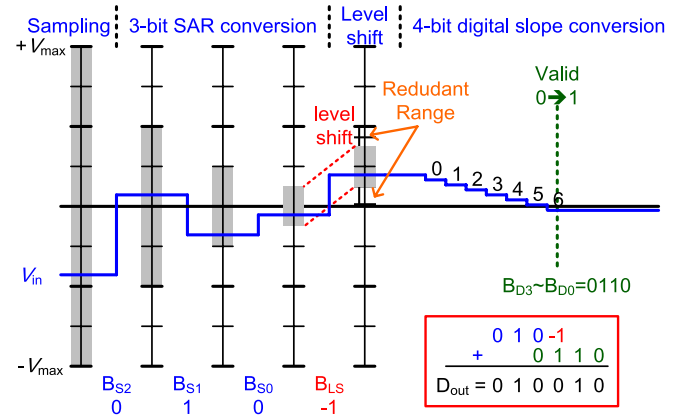

Fig. 4. A 6 bit operation example of the proposed SAR-assisted digital-slope ADC.

and fine ADCs into binary codes. The coarse SAR ADC and fine digital-slope ADC share a capacitor digital-to-analog converter (DAC). Therefore, there is no gain error between the coarse and fine ADCs. This hybrid architecture consists of only elementary analog circuits and digital blocks, making it attractive for advanced CMOS processes.

C. Operation Example of Proposed Hybrid ADC

Fig. 4 shows a 6 bit example to explain the operation of the proposed hybrid ADC. The 6 bit ADC consists of a 3 bit coarse SAR ADC and a 4 bit fine digital-slope ADC; there is a 1 bit redundancy overlap between the ADCs. After 3 bit SAR ADC conversion, the residue signal converges to the range of $[-V_{max}/8, +V_{max}/8]$. Next, the residue signal is level-shifted to the middle of the range $[0, +V_{max}/2]$ for the 4 bit digital-slope ADC conversion. After the residue signal has well-settled, the residue signal is continuously switched down with a 1 LSB step. When the residue signal is less than zero, the output of the CT-CMP changes polarity and stops the conversion of the fine digital-slope ADC. To obtain a correct output code, the offset induced by the redundant range is subtracted from the raw codes by the correction logic. The offset is four LSBs in this example.

D. Comparison With SAR-Assisted Zero-Crossing Pipelined ADC

To a certain extent, the proposed hybrid ADC is similar to a SAR-assisted zero-crossing pipelined ADC [16]. In fact, the operation of a multiplying DAC (MDAC) and back-end stages in a SAR-assisted zero-crossing pipeline ADC is replaced by the digital-slope operation in the proposed hybrid ADC. The digital-slope operation replaces the current source in the zero-crossing MDAC by digital ramping and directly quantizes the residue signal in the time domain, where the conversion time of the zero-crossing MDAC is proportional to the residue signal. With the digital-slope operation, the proposed ADC does not need the back-end stages required in a zero-crossing pipelined ADC, and hence has smaller power consumption and area.

III. Implementation of Proposed SAR ADC and Building Blocks

A. Proposed 12 bit SAR-Assisted Digital-Slope ADC

Fig. 5 depicts the building blocks of the proposed 12 bit SAR-assisted digital-slope ADC. The ADC samples the input signals at the top plates of capacitor arrays to reduce the number of unit capacitors by half. The sampling time is around 2.5 ns, which is 25% of a clock cycle. The coarse SAR ADC takes 8 bit cycles to convert 7 bits. Based on the redundant weighting method [17], the capacitor sizes from the first to the eighth MSB bits are 480, 256, 128, 64, 40, 24, 16, and 8 units, respectively. The capacitor DAC adopts a monotonic switching procedure [18] to reduce the switching power and simplify the control logic. The SAR ADC conversion takes about 2.4 ns. When the SAR ADC conversion finishes, capacitors C_{D15} to C_{D0} at the negative input terminal of the comparator are switched from V_{ref} to ground. The level-shift operation ensures that the residue voltage is within 25% to 75% of the input range of the digital-slope ADC. At the same time, the CT-CMP is enabled and its output is initially low. It takes about 0.8 ns for the capacitor DAC and CT-CMP to settle. Next, the delay line is enabled to start the conversion of the digital-slope ADC. Capacitors C_{D31} to C_{D0} at the positive terminal of the comparator are switched from V_{ref} to ground in sequence with an interval of 100 ps. When the voltage at the positive terminal is lower than that at the negative terminal, the output of the CT-CMP rises from low to high to stop the propagation in the delay line and disable the CT-CMP. At the same time, the time-domain information in delay cells is sampled by D-flip-flops, and the encoder converts the thermometer code into binary codes. The digital error correction (DEC) circuit converts the 14 bit redundant codes (8 bit codes from the SAR ADC and 6 bit binary codes from the digital-slope ADC) into 12 bit binary codes. This hybrid ADC does not need gain calibration because the coarse SAR ADC and the fine digital-slope ADC share a capacitor array.

The digital-slope ADC conversion in this work is single-ended, so it employs a unit capacitor that is twice as large as that for a differential ADC to perform 1 LSB switching [14]. The single-ended operation reduces the overall capacitor count by 2. After the 7 bit coarse SAR ADC conversion, the residue signal swing is around 12.5 $mV_{p\text{-}p}$ for a 1.6 $V_{p\text{-}p}$ ADC input signal swing. The single-ended operation induces a 6.25 mV input common-mode (CM) voltage (V_{cm}) variation in the CT-CMP. According to simulation, a 6.25 mV input variation of V_{cm} only causes a 2.7 ps delay uncertainty in the output signal generation of the CT-CMP. The difference

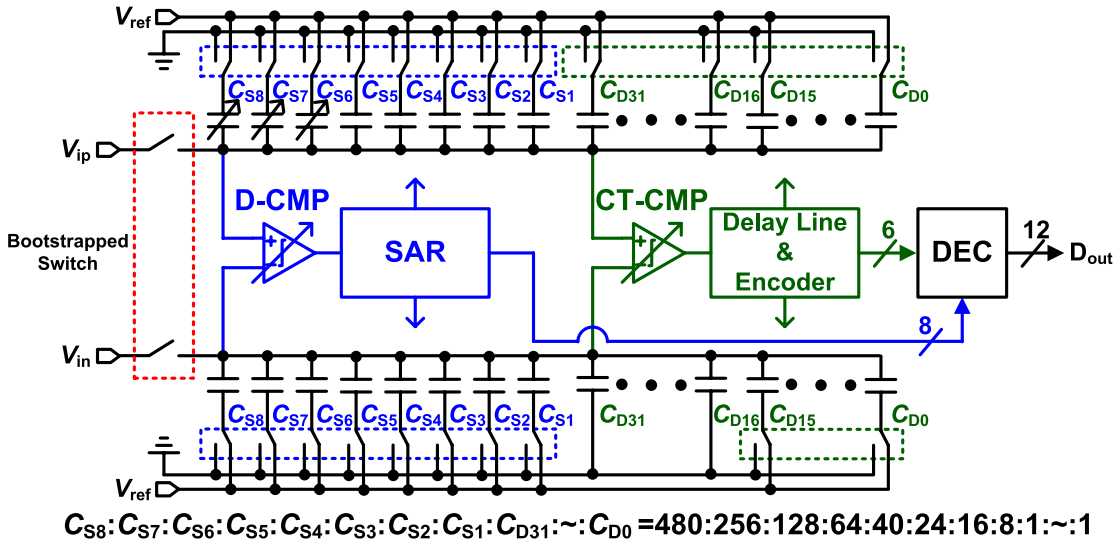

Fig. 5. Block diagram of the proposed 12 bit SAR-assisted digital-slope ADC.

TABLE I
ADC NOISE BUDGET

	Simulation Results	Noise Ratio
Sampling Noise	1 e-8 [V²]	16.3 %
Quantization Noise	1.27 e-8 [V²]	20.8 %
CT-CMP Noise	2.25 e-8 [V²]	36.8 %
On-chip Buffer Noise	1.6 e-8 [V²]	26.1 %
Total Noise	6.12 e-8 [V²]	100 %
SNR	67.2 [dB]	

is equivalent to 0.054 LSB and has a minor influence on the ADC conversion.

The *kT/C* noise of the sampling capacitor, quantization noise, CT-CMP noise, and on-chip reference buffer noise totally yielded a 67.2 dB SNR. Table I summarizes the detailed noise breakdown of the prototype hybrid ADC. The CT-CMP noise was obtained by calculating the jitter of the CT-CMP output with a transient noise simulation. The on-chip reference buffer noise was obtained by integrating the output noise with a noise simulation. The overall noise is signal-independent.

B. Continuous-Time Comparator

Fig. 6 depicts a schematic of the CT-CMP, which uses a two-stage structure to increase the open-loop gain. The inverter guarantees that the output signal will produce logic levels for the succeeding digital circuit. For proper function with an input CM voltage of around 100 mV, the CT-CMP uses a p-type input pair for the first stage, and an n-type input pair for the second stage. Some MOS capacitors are added to decouple the gate bias of the current sources. The decoupling capacitors are designed to be 8 times the size of the current sources.

The CT-CMP turns off to save power during the sampling phase, SAR ADC conversion, and idle time after the

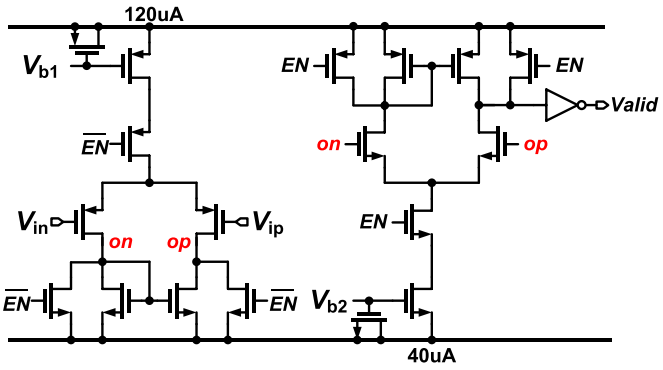

Fig. 6. Schematic of a low-noise low-power CT-CMP.

digital-slope ADC conversion. When the CT-CMP turns on, the first and second stages consume only 120 and 40 μA, respectively. Before the digital-slope ADC conversion, the CT-CMP takes about 0.8 ns to settle, which prevents the digital-slope ADC conversion from experiencing startup transients. The CT-CMP is designed to have a very low bandwidth (the -3 dB bandwidth is designed to be around 100 MHz) that is much lower than the 10 GHz step frequency (an interval of 100 ps) of capacitor switching. The low-bandwidth CT-CMP filters out high-frequency harmonics and noise of the stair curve, and uses the low-frequency components and noise to generate the output signal. Fig. 7 shows a mathematical concept to explain the effectiveness of the low-bandwidth CT-CMP. Fig. 7(a) plots a stair step curve with an interval of ΔT, which is the input signal of the CT-CMP. Fig. 7(b) shows a fast Fourier transform (FFT) spectrum of the stair step curve. The step frequency is the inverse of ΔT. The low-bandwidth CT-CMP acts as a low-pass filter (LPF), attenuating the high-frequency components. Fig. 7(c) shows the effective spectrum after filtering by the low-bandwidth CT-CMP. Taking the inverse FFT of the effective spectrum, we can get the equivalent input signal curve of the low-bandwidth CT-CMP, as shown in Fig. 7(d). With the low-bandwidth CT-CMP, the switching capacitor curve is similar to discharging with a

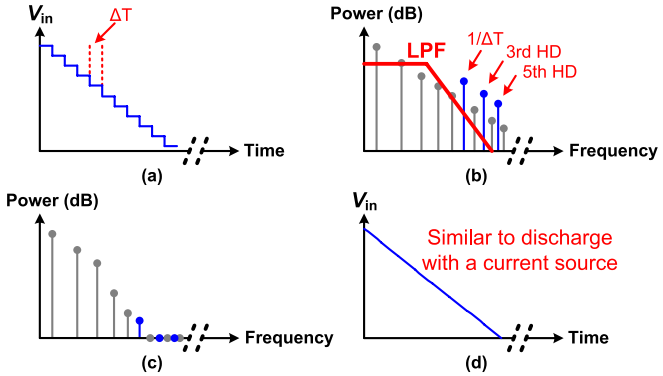

Fig. 7. (a) Stair step curve with an interval of ΔT. (b) FFT spectrum of the stair step curve. (c) Effective spectrum after fitlering by the low-bandwidth CT-CMP. (d) Equivalent input signal curve of the low-bandwidth CT-CMP.

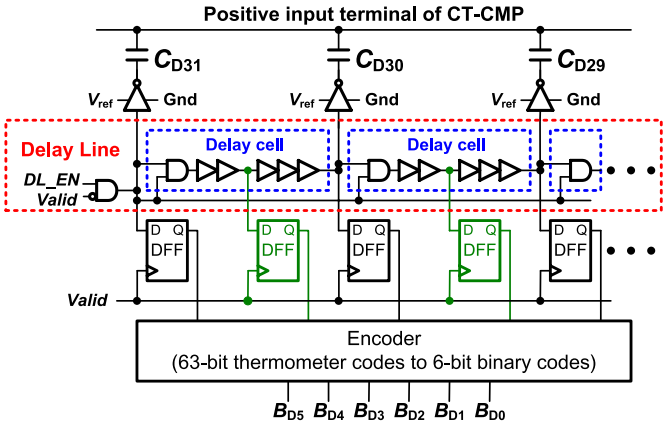

Fig. 8. Implementation of the 6 bit digital-slope fine ADC.

current source in a dual-slope ADC. The low bandwidth alleviates the signal-dependent effect and makes the comparison time more linearly proportional to the input voltage. Therefore, the digital-slope ADC can achieve a higher resolution using time-domain interpolation without extra unit capacitors.

Using the CT-CMP for the LSBs conversion has some benefits compared to using a dynamic comparator. First, it only needs one comparison for N-bit conversions and is free of the metastability problem. Second, it works like an integrator and takes a much longer comparison time to generate the output. Therefore, it has better suppression of high-frequency noise. In this work, the input-referred noise of the CT-CMP is designed to be 150 μV. If we designed a dynamic comparator [17] with roughly $1/N$ the energy consumption of this CT-CMP, its input-referred noise would be up to 360 μV according to simulation. The CT-CMP thus achieves better efficiency in suppressing noise.

C. Fine Digital-Slope ADC With Time-Domain Interpolation

Fig. 8 shows the implementation of the 6 bit fine digital-slope ADC, which consists of delay cells, switches, unit capacitors, D-flip-flops, and an encoder. Except for the unit capacitors, all components are constructed using digital standard library logic cells, which are provided by a foundry and have verified device properties and a regular and compact layout size. Each delay cell consists of an AND gate and five buffers. The six logic gates have a total delay time of around 100 ps. With the help of the low-bandwidth CT-CMP, an additional bit is generated by time-domain interpolation. With interpolation, the LSB time step in this design is equivalent to 50 ps. According to simulation results, random mismatch results in a standard deviation of 2.0 ps for the delay of each delay cell. The standard deviation of the maximum integral nonlinearity (INL) in a thermometer DAC can be expressed as [19]

$$\sigma_{\max \mathrm{INL},}(\mathrm{LSB}) = 0.5\sqrt{n} * \sigma \tag{3}$$

where n is the total number of unit cells. With 32 delay cells, the standard deviation of the maximum INL is 5.66 ps. In addition, according to transient noise simulation, the circuit noise results in a standard deviation of only 193 fs in different cycles. These variations are much smaller than a 1-LSB time step. Therefore, the random mismatch and noise of the delay cells have a minor influence on the SNR.

During the digital-slope approaching (switching at most 32 times), the fine ADC obtains 63 samples using D flip-flops when the *Valid* signal goes high. The encoder converts the 63 bit thermometer codes into 6 bit Gray codes, and then converts the 6 bit Gray codes into binary codes. For a 6 bit digital-slope ADC, 1 bit time-domain interpolation helps to reduce the total number of unit capacitors from 64 to 32, which reduces the hardware complexity by a factor of 2. The parasitic capacitance of the routing line is much greater than the unit capacitance. Reducing the total number of routing lines thus reduces the circuit area and switching power consumption caused by parasitic capacitance. The ADC can achieve a higher SNR with more aggressive time-domain interpolation (e.g., 2 or 3 interpolated samples between two switching nodes) at the cost of increasing the number of D-flip-flops and the complexity of the encoder.

D. Latency Compensation

Fig. 9 plots a diagram of the latency from the crossing-point generation of the *Valid* signal in the low-bandwidth CT-CMP. The latency problem here is similar to that of a zero-crossing pipelined ADC. However, the latency is harmful to zero-crossing pipelined ADCs because the current source in a zero-crossing-based circuit (ZCBC) MDAC has limited linearity, resulting in a signal-dependent offset for the conversion even if the latency is well-compensated. Owing to the intrinsic high linearity of digital ramping, the latency in this work results in only a constant systematic offset. The latency can be compensated by additional delay cells and removed in the digital domain by estimating the offset according to post-layout simulation. Fig. 10 shows the implementation of latency compensation. The additional delay cells are designed with a delay of 100 ps, which is the same as that of the first 32 delay cells. The number of additional delay cells depends on the latency. To remove the latency in the digital domain, the sampling positions of the D-flip-flops are shifted according to the number of additional delay cells. In this way, the latency is easily removed from the ADC conversion.

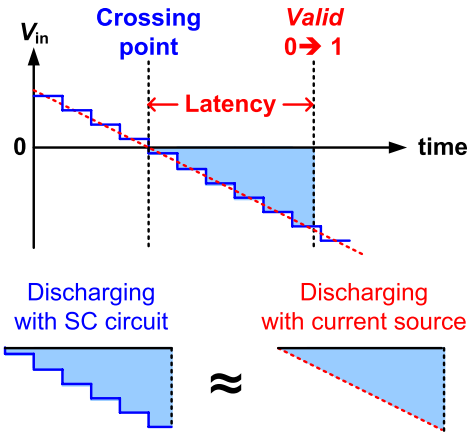

Fig. 9. The latency from the input crossing point to the *valid* signal generation.

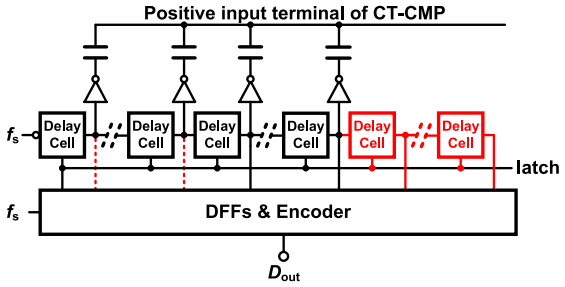

Fig. 10. Implementation of latency compensation.

The mismatch between the latency of the CT-CMP and the total delay of the additional delay cells in PVT corners can be compensated with CT-CMP offset calibration, which is mentioned in Section III-F.

E. On-Chip Reference Voltage Buffer

For a SAR ADC with a 100 MS/s sampling rate, the capacitor DAC network must settle in a few hundred picoseconds or less, which requires a high-speed reference buffer, especially for the MSB cycle. With the help of the redundant algorithm [17], the bandwidth requirement of the reference buffer can be relaxed greatly. An open-loop source-follower architecture is adopted for the proposed ADC, as shown in Fig. 11. The $V_{BG}$is equal to 0.9 V, which tracks the bandgap voltage and is insensitive to temperature and process variation. In order to generate an output voltage V_{ref} of 0.9 V, the resistance ratio of R1/R2 is designed to be equal to the NMOS size ratio of M2/M1. R0 and C0 act as a low-pass filter to isolate the kick-back noise from the ADC. The open-loop topology has the benefits of small output impedance (which is equal to $(1/gm_2)$//R2), wide bandwidth, and small area. It is very suitable for high-speed operation.

F. Non-ideal Effect of Proposed ADC

The performance of the proposed ADC may degrade due to a lot of nonideal effects, such as device mismatch and power supply noise. These nonideal effects must be carefully dealt with to ensure that the ADC works properly without performance degradation.

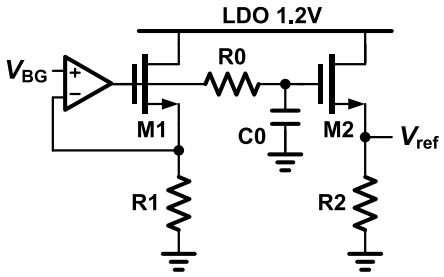

Fig. 11. Schematic of reference buffer.

Although the redundancy between the coarse SAR ADC and fine digital-slope ADC can tolerate their offset mismatch, it is insufficient when a small comparator size is used. To make the design more robust, the input offsets of the D-CMP and the CT-CMP are calibrated in the foreground by shorting the inputs to V_{cm}. Dynamic offset caused by temperature and supply voltage variations can be tolerated by the 16-LSB redundant range in this design. If the redundant range is insufficient for a critical case, the 6-bit output of the digital-slope ADC will contain the boundary codes (0 or 63). The offset of the CT-CMP can be adjusted in the background to ensure that the 6 bit output code is within the range of 0 to 63 by utilizing boundary code detection logic.

The first 3 MSB capacitors in the capacitor array at the positive terminal are also calibrated in the foreground with a step size of 0.5 LSB and a range of 4 LSB. The calibration mechanism is similar to a previously reported one [20]. Instead of adjusting the bit weights and generating the digital output in the digital domain, we adjust the capacitances to match the ideal bit weights in the analog domain to avoid extra digital power consumption. However, the accuracy is limited by the finite step size, and the error will propagate with the calibration of each capacitance. Therefore, we only calibrate the first 3 MSB capacitances, and enhance the LSB capacitors matching by placing them together in the center of the DAC network to achieve 9 bit linearity.

The static PVT variation leads to a static offset for the ADC that can be compensated with CT-CMP offset compensation. However, the dynamic variations at the input CM and supply voltage will degrade ADC performance. According to the simulation, the CM rejection ratio of the ADC is 49.5 dB (a 100 V input CM variation results in an input-referred offset of 0.336 mV). The power supply rejection ratio of the ADC is 36.0 dB (a 100 mV supply variation results in an input-referred offset of 1.857 mV). The CM rejection ratio can be improved by enlarging or cascading the current source of first stage in the CT-CMP, which would lead to a more constant current for different input CM voltages. The power supply rejection ratio can be improved by reducing the latency of the CT-CMP, while it consumes more power to improve the bandwidth of CT-CMP. In this work, a 0.9 V low-dropout regulator is used to supply the proposed ADC to avoid interference from other circuits.

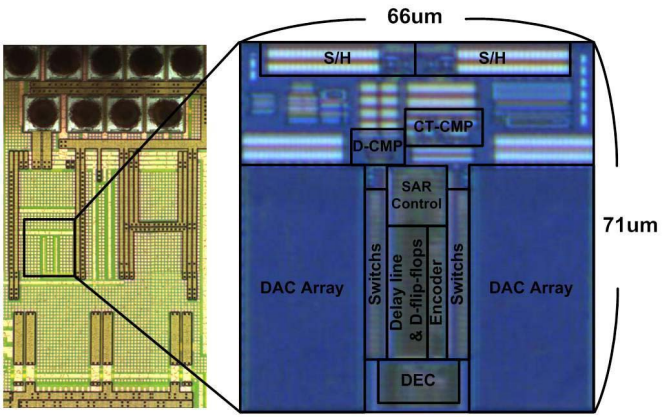

Fig. 12. Chip micrograph and delayered zoomed-in view of ADC core.

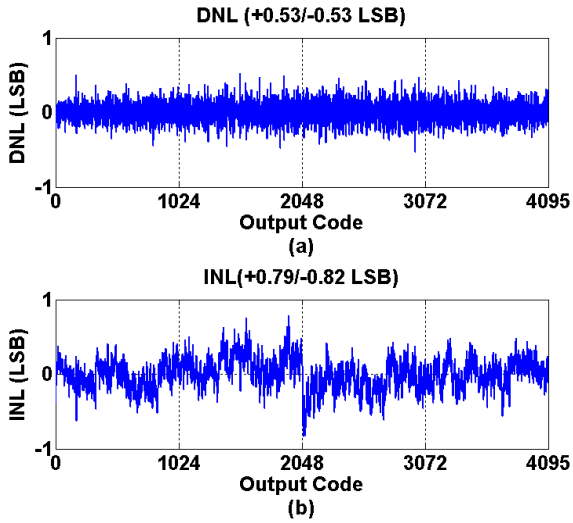

Fig. 13. Measured static performance. (a) DNL. (b) INL.

There is a serious non-ideal effect when using an on-chip reference buffer. The number of unit capacitors connected to the reference voltage depends on the input signal after the SAR operation. The digital ramping sinks a signal-dependent current from the reference buffer during the digital-slope ADC conversion. The output impedance of the reference buffer generates a signal-dependent drop in the reference voltage, which causes a bowing effect on ADC conversion, which is similar to the problem in zero-crossing pipelined ADCs [21]. This problem can be alleviated by enlarging the output stage current to reduce the output impedance, or adding a replica cross-coupled capacitor DAC for current compensation [21].

IV. Measurement Results

A prototype was fabricated in one-poly eight-metal (1P8M) 28 nm HPM CMOS technology. A chip micrograph and a delayered magnified view of the ADC core are shown in Fig. 12. The ADC core occupies an active area of 66 μm $\times$ 71 μm. The unit capacitance in the capacitor DAC is 0.8 fF. The total sampling capacitance of the single-ended capacitor network is 0.9 pF. The measurement results of the prototype are presented below.

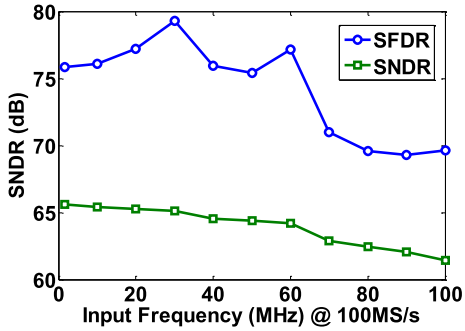

Fig. 14. Measured dynamic performance versus input frequency at 0.9 V and 100 MS/s.

A. Static Performance

The static performance of the proposed ADC was evaluated with a 0.9 V supply and a 100 MS/s sampling rate and an input signal frequency of close to 1 MHz. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 14. The peak DNL and INL are +0.53 / 0.53 LSB and +0.79 / 0.83 LSB, respectively.

B. Dynamic Performance

Fig. 14 shows a plot of the measured SFDR and SNDR versus the input frequency with 0.9 V and 100 MS/s. At a low input frequency, the measured SNDR and SFDR are 65.67 and 75.87 dB, respectively. The resultant effective number of bits (ENOB) is 10.62 bits. When the input frequency is increased to the Nyquist frequency, the measured SNDR and SFDR are 64.43 and 75.42 dB, respectively. The resultant ENOB is 10.41 bits. The effective resolution bandwidth (ERBW) is around 80 MHz and the SNDR is still greater than 60 dB when the input frequency is increased to 100 MHz.

Fig. 15 shows a plot of the measured FFT spectrum with a Nyquist frequency input. The second and third harmonics mainly result from the output impedance of the on-chip reference buffer, as mentioned in Section III-F.

C. Power Consumption

With a 100 MS/s sampling rate, the ADC consumes a total power of 0.35 mW from a 0.9 V supply and a 0.9 V reference. The power consumption breakdown is shown in Fig. 16. The analog blocks consume 34% of the total power, including 64 μW for the S/H circuit and the D-CMP, and 56 μW for the CT-CMP. The digital blocks consume 41% of the total power, including 70 μW for the delay line, D flip-flops, and encoder, 53 μW for the SAR control logic, and 21 μW for the DEC logic. The power dissipation of the capacitor DAC and the leakage current are 80 and 6 μW, respectively.

In this work, the power consumption of the reference buffer was not optimized. The current of the reference buffer was just increased to alleviate the bowing effect. The on-chip reference buffer occupies an area of 70 μm $\times$ 40 μm and consumes up to 1.56 mW of power, which is much higher than that

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCS

	This Work	ISSCC 2014 [9]	VLSI 2014 [10]	ISSCC 2015 [12]	VLSI 2015 [22]
Technology	28 nm CMOS	28 nm CMOS	28 nm CMOS	65 nm CMOS	14 nm CMOS
Architecture	SAR-assisted Digital Slope	SAR-assisted Pipelined	SAR-assisted Pipelined	SAR-assisted Pipelined	SAR
Supply [V]	0.9	1.0	0.9	1.2	1.2
Resolution [Bit]	12	14	14	13	12
Fs [Ms/s]	100	80 (2 CHs)	200 (2 CHs)	50	70
Input Swing [Vpp]	1.6	1.4	--	2.4	1.6
Sampling Capacitance [pF]	0.9	1.4	3.5	2.0	--
SNDR@Low Frequency [dB]	65.67	68	70	71.5	69
SNDR@Nyquist [dB]	64.43	66	65	70.9	68.1
Power [mW]	0.35	1.5 (1.2**)	2.3	1.0	4.3
$FOM_{W,lf}$ [fJ/conversion-step]	2.2	9.1 (7.3**)	4.4	6.5	26.7
$FOM_{W,hf}$ [fJ/conversion-step]	2.6	11.5 (9.2**)	7.9	6.9	29.6
$FOM_{S,lf}$ [dB]	177.2	172.3 (173.3**)	176.4	175.5	168.1
$FOM_{S,hf}$ [dB]	176.0	170.3 (171.3**)	171.4	174.9	167.2
Active Area [mm^2]	0.0047	0.137	0.1	0.054	0.019
Calibration	Yes (offset, DAC)	Yes (gain, offset, DAC)	Yes (gain, offset, DAC)	No	Yes (DAC)
Reference Buffer Included?	No*	Yes	No	No	No

*Reference buffer is realized on-chip, but the area and static power is not included in the calculation.
**Removed the reference buffer power consumption form the calculation.

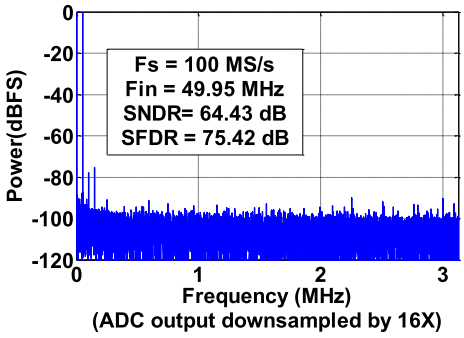

Fig. 15. FFT plot with input frequency close to Nyquist frequency.

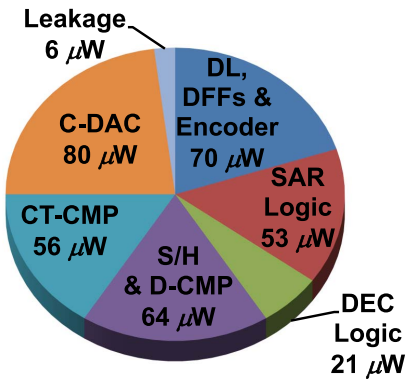

Fig. 16. Power consumption breakdown.

consumed by the proposed ADC. If the reference buffer is optimized by adding a replica cross-coupled capacitor DAC for current compensation [21], its power consumption can be reduced to 0.4 mW according to simulation.

D. Performance Summary and Comparison

The Walden and Schreier FoM equations are defined, respectively, in

$$FoM_W = \frac{Power}{2^{ENOB} \times f_S} \tag{4}$$

$$FoM_S = SNDR + 10\log\left(\frac{f_S}{2 \times Power}\right) \tag{5}$$

where f_S is the sampling frequency. At low input frequency, the Walden and Schreier FoMs are 2.2 fJ/conversion-step and 177.2 dB, respectively. At the Nyquist input frequency, the Walden and Schreier FoMs are 2.6 fJ/conversion-step and 176.0 dB, respectively. Table II summarizes the ADC performance and compares the proposed design to published ADCs with comparable sampling rates and resolutions [9], [10], [12], [22]. Only one published work [10] used an on-chip reference buffer, the other works [9], [12], [22] used large on-chip decoupling capacitances to stabilize the reference voltage. It is unfair to compare these different designs because the on-chip reference buffer consumes static power and contributes extra noise to the ADC. Therefore, we

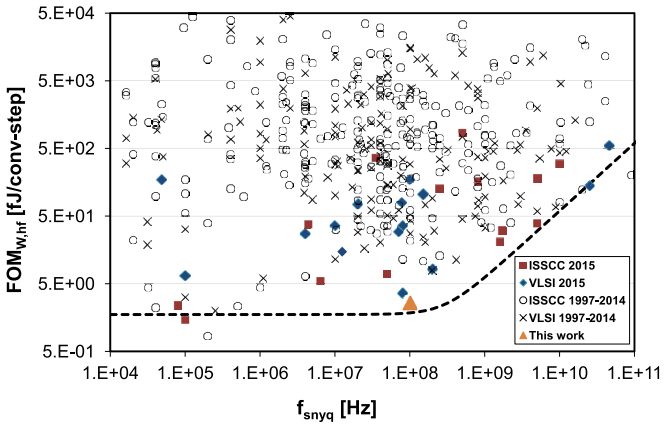

Fig. 17. Comparision of Walden FoM with the ADCs presented at ISSCC and VLSI between 1997 and 2015 [23].

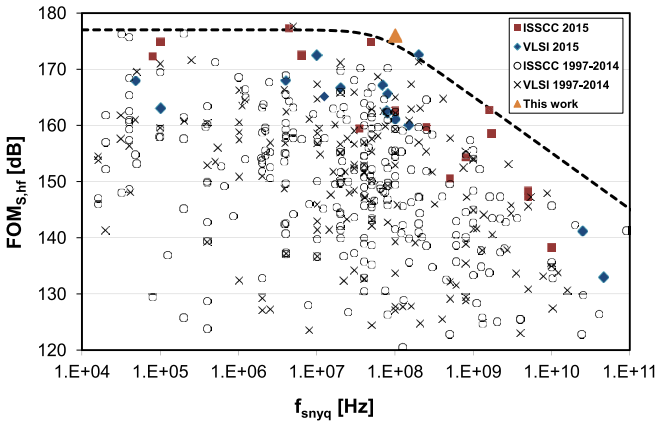

Fig. 18. Comparision of Schreier FoM with the ADCs presented at ISSCC and VLSI between 1997 and 2015 [23].

list the performance in brackets for [10], which does not take the reference buffer power into account.

Figs. 17 and 18 plot the Walden and Schreier FoMs of the ADCs presented at ISSCC and VLSI between 1997 and 2015 [23]. The proposed design has the best Walden and Schreier FoMs among ADCs with sampling rates of higher than 10 MS/s. In addition, the ADC active area is at least 4 times smaller than those of published ADCs with resolutions of higher than 12 bits [23].

V. Conclusion

This paper proposed a hybrid ADC architecture that combines the advantages of the SAR ADC and the digital-slope ADC. A 7 bit low-power coarse SAR ADC is used to fast approach the input signal. A 6 bit low-noise fine digital-slope ADC is used to linearly approach the small residue signal of the coarse ADC. A time-domain interpolation technique is used to increase the resolution and prevent the digital-slope ADC from using a small unit capacitance.

The prototype of the proposed design fabricated in 28 nm CMOS technology has a 100 MS/s sampling rate and an ENOB of 10.41 bits. It only consumes 0.35 mW of power and occupies an active area of 66 μm $\times$ 71 μm. The experimental results demonstrate the power and hardware efficiency of the proposed hybrid ADC.

Acknowledgement

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