A 20-ch TDC/ADC Hybrid Architecture LiDAR SoC for 240 × 96 Pixel 200-m Range Imaging With Smart Accumulation Technique and Residue Quantizing SAR ADC

Kentaro Yoshioka[®], Hiroshi Kubota, Tomonori Fukushima, Satoshi Kondo, Tuan Thanh Ta[®], *Member, IEEE*, Hidenori Okuni, Kaori Watanabe, Masatoshi Hirono[®], Yoshinari Ojima, Katsuyuki Kimura, Sohichiroh Hosoda, Yutaka Ota, Tomohiro Koizumi, Naoyuki Kawabe, Yasuhiro Ishii, Yoichiro Iwagami, Seitaro Yagi,

Isao Fujisawa, Nobuo Kano, Tomohiko Sugimoto, Daisuke Kurose, Member, IEEE,

Naoya Waki, Yumi Higashi, Tetsuya Nakamura, Yoshikazu Nagashima,

Hirotomo Ishii, Akihide Sai¹⁰, and Nobu Matsumoto

Abstract—This presents time-to-digital paper a converter/analog-to-digital-converter (TDC/ADC) hybrid LiDAR system-on-chip (SoC) to realize reliable self-driving systems. The smart accumulation technique (SAT) is proposed to achieve both 200-m and high-pixel-resolution range imaging, which was untrodden with conventional LiDARs. The "smart" accumulation is realized by a simple object recognition strategy with small circuit overhead. When compared to conventional accumulations, the LiDAR range is enhanced without degrading the pixel resolution. Moreover, a TDC/ADC hybrid architecture is proposed to achieve a wide-distance-range LiDAR with a small silicon area and short-range precision. To minimize the ADC cost, a residue-quantizing noise-shaping (RQNS) SAR ADC is proposed. The prototype LiDAR SoC is fabricated in the 28-nm CMOS technology and integrated into the silicon photomultiplier (SiPM)-based LiDAR system. LiDAR measured with 240 × 96 pixels at 10 frames/s achieves a measurement range of 200 m with a 70-klx direct sunlight: the measurement range is 2x longer than conventional designs. Furthermore, our LiDAR achieves 4× higher effective pixel resolution compared to conventional designs using simple accumulation. A 3-D point-cloud image acquired with a real-life environment is presented.

Index Terms—Direct time of flight (DToF), LiDAR, range measurement, SAR analog-to-digital-converter (ADC), smart accumulation technique (SAT), TDC/ADC hybrid, ToF.

I. INTRODUCTION

S ELF-DRIVEN cars can ultimately reduce or even eliminate car accidents and traffic jams. The ability of sensors to measure long ranges (LRs) (up to 200 m) as well as high image quality and resolution are essential to provide safe and reliable self-driving programs of Level 4 and above [1]. Considering that the braking distance when traveling at

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The authors are with Toshiba Corporation, Kawasaki 212-8582, Japan (e-mail: yoshioka@iskr.elec.keio.ac.jp).

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120 km/h or 75 mi/h is 150 m on highways, sensing range of 200 m is required to detect preceding vehicles with a sufficient margin. Moreover, in order to realize safe and reliable self-driving in urban areas, sensors uniting wide angleof-view and high-pixel resolution are required to fully perceive the surrounding events and securely detect pedestrians. It is challenging for the conventional sensors to cover these requirements, millimeter radars measure long distances but its resolution is limited [2] and have trouble resolving accurate distances. Furthermore, optical cameras have difficulty resolving depth [3].

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LiDAR, on the other hand, can achieve both fine image resolution and depth perception using time of flight (ToF). The major weak point of LiDAR, a poor robustness for weather condition, e.g., rain, snow, and fog, should be compensated by sensor fusions, such as millimeter-wave radars + LiDARs.

This paper further explains the LiDAR system-onchip (SoC) presented in ISSCC 2018 [15]. This paper is organized as follows.

- 1) Tutorial coverage on the state-of-the-art LiDAR architecture. Here, we define LiDAR signal-to-background photon ratio (SBR) (Section II).
- 2) Details and analysis on the proposed smart accumulation technique (SAT) (Section III).
- 3) LiDAR hardware architecture discussions (Section IV).
- 4) Circuit implementation details (Section V).
- 5) Measurement results including 3-D point-cloud images (Section VI).

II. LIDAR SYSTEM ARCHITECTURE

A. ToF Architecture

There are mainly two types of photodetectors (PDs) used for ToF measurements: a linear-mode avalanche photodiode (APD) which has relatively low-gain and high-gain Geiger-mode operated APD with quenching circuits also known as single-photon avalanche diode (SPAD) [19]. In this paper, we utilize silicon photomultipliers (SiPM) [20],

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Fig. 1. DToF LiDAR operation. The distance to the object is directly obtained by measuring the ToF of the laser photon.

which connect multiple SPADs in parallel to minimize the printed circuit board footprints.

LiDARs are based on mainly two types of ToF detection techniques, indirect ToF (IToF) [16]-[18] and direct ToF (DToF) [4]-[15]. IToF is based on a modulation and demodulation of laser amplitude or phase. The phase difference between the output of the laser and reflection is detected by the PD. The detected phase difference is stored as a charge and calculated as a ToF by sampling using an ADC. This method can achieve high image resolutions. IToF is, however, not suitable for LR measurement. This is because the linear-mode APD, required to achieve the highly linear time-to-charge conversion, has magnitudes lower sensitivity than SPADs/SiPMs. On the other hand, DToF is suitable for LR measurement; the returned laser pulse is detected by a high-sensitivity SiPM (Fig. 1) and is capable of detecting even single-photon inputs. Since LR measurement is crucial in our application, we build upon the DToF architecture with a 2-D scanning mechanism, further explained in Section II-B.

B. LiDAR Scanning Systems

With a large 2-D SPAD array, the LiDAR can operate similar to an image sensor, the entire distance image can be acquired without scanning (flash LiDAR) [11]–[13]. While the silicon front-end design is challenging, flash LiDAR can omit the expensive mechanical and optical components for scanning; the LiDAR system becomes low cost. Although, its performance is fundamentally limited since laser photons must be distributed to thousands of pixels. Therefore, the available laser photons/pixel is low, and the performance does not reach the requirement of self-driving systems.

By utilizing a scanning system in LiDARs, the performance can be greatly improved with the added expense of the scanning components. While single point (or single pixel) measured LiDARs can make the best use of laser photons and resolve long distances, the frame rate per second (FPS) is constrained by the large number of scans required to construct the whole image. Therefore, in order to leverage the balance between FPS and laser photon use, advanced driver-assistance systems (ADAS) LiDARs acquire multiple pixels at each measurement and conduct a 2-D scan through the imaging space via polygon mirrors [4]–[6].

Fig. 2 further shows the 2-D column scan conducted in our LiDAR system. First, the LiDAR acquires 20 column pixels



Fig. 2. 2-D multi-column scanning done in the LiDAR system to obtain a single image (or frame). In each measurement, 20 column pixels are acquired.

with a single measurement where a horizontal scan is executed to acquire the image space of row#1, represented by the red arrow in Fig. 2. When the first horizontal scan is finished, scanning row#2 is executed, which is indicated by the blue arrow. This procedure is repeated until the whole image is acquired, where we indicate the fully scanned image as a frame. In our LiDAR system, 10 frames are acquired per second, and each ToF measurement takes about 4.5 μ s. The horizontal pixel resolution can be flexible from 1920 to 240 pixels based on the tradeoff between resolution and distance.

The mechanical and optical components required for laser scanning greatly limit the LiDAR's cost, size, and reliability. To counter this problem, use of MEMS mirror [7], [8] and optical phased mirror [9], [10] are explored to shrink the scanning system. While these technologies can bring a significant breakthrough to LiDAR applications, their optical loss is still too large to replace the polygon mirror.

C. Defining LiDAR SBR

In this paper, we will utilize LiDAR SBR to discuss the performance of DToF LiDARs. Since we do not include the effects of sampling and the statistical behavior of photons, (1) is not rigid. We would like to emphasize that the goal of defining LiDAR SBR is to discuss the effects of noise photons in LiDAR systems, so relative effects can be discussed conveniently in this paper

$$= \log_{20} \frac{\text{Number of laser photons detected@SiPM}}{\text{Number of background photons detected@SiPM}}.$$
(1)

The numerator indicates the number of detected laser photons when measuring at a particular distance. The denominator shows the number of background photons detected, which in ADAS LiDARs, the largest source is the sunlight, since we cannot distinguish that the incoming photon is either sunlight or laser (even with optical bandpass filters). Other noise sources, e.g., SiPM darkcount, afterpulse, and circuit noise, are magnitudes lower and thus neglected in this analysis. Importantly, laser light diffuses as it propagates through air: the signal loss follows the inverse square law against distance in LiDARs. Only one-fourth of photons is returned from 200-m ranged targets when compared with targets 100 m away. (The SBR is 12 dB worse.) Therefore,



Fig. 3. Laser and SiPM output waveforms are shown, where 200-m DM is conducted under strong sunlight.



Fig. 4. Accumulation done by a 3×3 accumulation window is illustrated. To centered pixel E, the neighboring data (A–I) are accumulated. Imaging such situation with simple accumulations is challenging.

the LiDAR SBR is strictest during 200-m LR measurements with daylight, especially at sunset when the sunlight intensity can reach 100 klx. Fig. 3 shows an example of a SiPM output when a measurement is conducted at such conditions. Note that due to strong sunlight, background light-induced photons may pile up and generate a higher SiPM current peak than the returned laser pulse. Since peak detection will easily fail in such conditions, an accumulation technique, as discussed in Section II-D, is mandatory to enhance the SBR.

Note that our system utilizes laser wavelength of 905 nm. By moving to lasers with 1550-nm wavelength, the sunlight photons can be reduced significantly with expensive nonsilicon PDs.

D. Simple Accumulation and Its Drawbacks

How can we improve the LiDAR SBR using algorithmic techniques? An effective method is pixel accumulation (averaging). Conventional LiDARs [4] utilize two types of pixel accumulation: 1) by accumulating multiple measurements within the same pixel (or temporal averaging) and 2) accumulating the results of neighboring pixels (NPs) (or spatial averaging). Both accumulation methods improve the LiDAR SBR by the square root of accumulated samples. However, the prior method has a tradeoff between FPS. To further improve the SBR without degrading FPS, Niclass *et al.* [4] utilizes the spatial accumulation method, where we refer to as "simple" accumulation.

The simple accumulation is only effective when the accumulated pixels all "watch" the same target. If a pixel is "watching" a different target, the image quality of the image will be degraded, which is further illustrated in Figs. 4 and 5. Here, we apply a 3×3 accumulation window to pixel E, to accumulate all NPs (A–I). As shown in Fig. 5, pixels D–I "watch" the same object (a car), and accumulation contributes to



Fig. 5. Processed waveforms with "simple" accumulation. Since SiPM outputs of two objects are accumulated, ToF measurement can be mistaken.



Fig. 6. LiDAR design tradeoffs.

enhancing the SBR. However, pixels A–C watch a different object (an electric pole); in cases where the distance and reflection rate greatly differs from the main target (a car), the reflected laser output amplitude and the ToF information seen at the SiPM waveform will be significantly different. Accumulated data may show two peaks, therefore easily failing the ToF measurement. Here, we would recognize that "simple" accumulation is similar to Blur algorithms; while denoising can be accomplished by spatial accumulations, object edges disappear and the image quality is degraded. In LiDARs, this leads to misdetection of small objects. Since it is crucial for the LiDARs to detect small objects, e.g., pedestrians, in self-driving systems, this cannot be overlooked.

III. SMART ACCUMULATION TECHNIQUE

A. Tradeoffs in LiDAR Design

We would like to wrap up the perspectives given at Section II as LiDAR design tradeoffs. Since the signal power or the laser power is limited by the eye safety in commercial LiDAR systems, we have a clear tradeoff between measurement distances versus the image quality, which is shown in Fig. 6. We can improve the measurement distance by utilizing simple accumulation, but the image quality is degraded by the "Blur" characteristic. Without accumulation, optimal image quality can be obtained but the LiDAR SBR is low: the measurable distance is insufficient for our self-driving target. The requirement is extremely strict for self-driving LiDARs, since we must fulfill both image quality and distance at a high level. The conventional technique would not let fulfill this target.

B. Concept of SAT

In order to accomplish the self-driving LiDAR target performance, we propose the SAT to break the performance tradeoff between the image quality and measurement distance. The SAT enhances the LiDAR SBR with minimum



Fig. 7. Concept of binary object classification with SAT explained with an example of image capturing of two objects.

image quality degradation, resulting in both long distance measurement (DM) and high image quality. To avoid the SBR degradation due to the accumulation of pixels watching different objects, SAT performs binary object classification before accumulation. Binary object classification determines whether a pixel is watching the same object as the referenced pixel or not; the pixel sets to accumulate if the same object is watched and ignored vice versa. The idea of SAT is similar to bilateral filters often used in image processing, which is an adaptive filter for edge preservation in denoising filters. To the best of our knowledge, SAT is the first to introduce adaptive filtering upon processing raw ADC result to enhance the precision of ToF measurement.

C. Algorithm of SAT

We will explain the algorithm of SAT with Fig. 7, where a car and electric pole are present. We will assume that E is the measuring pixel (MP), and the surrounding pixels are candidates for accumulation; thus, a 3×3 accumulation window is utilized. Remember that accumulation of the pixels D, F, G, H, and I "watching" the same target (a car) as E will contribute to the SBR improvement but accumulating others (pixels A, B, and C "watching" electric pole) can degrade the SBR. To prevent this problem, a binary object classification is done with SAT; the pixel data (the raw ADC output) are pre-processed, and the peak level (PL) and floor level (FL) are tagged as shown in Fig. 8. Note that the amplitude swing of the ADC depends on the number of captured photons, and hence PL has a strong correlation against the reflectivity and distance of the target. Moreover, FL also has a strong correlation against the target since the sunlight not only injects directly to the LiDAR but also comes in through the reflection of the target. SAT only accumulates the corresponding pixel when the correlation of both PL and FL against MP excesses appropriate value (Fig. 9). Utilizing both PL and FL for the target recognition, SAT enhances not only the accuracy but also the environmental robustness; the former is effective at daytime situation when FL is relatively high, and the latter is effective when sunlight level is relatively low.

D. Analysis of SAT

Here, we will focus on the analysis of SAT, especially on the 200-m DM results. As we have briefly stated, SAT will accumulate only NP data which has a high correlation to the targeting MP. Therefore, the LiDAR SBR is improved efficiently without degrading the image quality. The correlation between MP and NP is derived from the laser light amplitude: PL and environment light amplitude: FL.



Fig. 8. (a) Raw output of each pixels or the ADC output waveforms. When the pixels "watch" the same object, its PL and FL show high correlation and SAT will use such information to classify the objects. (b) With SAT, only the pixels "watching" the same object are accumulated; the SBR is improved significantly.



Fig. 9. SAT checks the correlation of PL and FL between the measured pixel and the pixel to be accumulated.

The possibility of MP and NP "watching" the same object has a non-linear relationship against the correlation derived from PL and FL, as shown in Fig. 10(a). Therefore, by setting the accumulation threshold to 0.5, the possibility of accumulating a different object than was, otherwise, expected can be reduced by $4 \times$ compared to "simple" accumulation. This leads to longer measurement range and higher image quality. Note that applying both PL and FL improves the possibility that data of same objects are accumulated. Fig. 10(b) shows a system simulation result where a 10% reflection target is placed. Also, non-target objects are generated with random distances to simulate real-life urban situations. To analyze the benefit of SAT, we vary the target size (plotted as $pixel^2$) in simulations (the target width-height is randomized as well). Here, we evaluate the measurement as "success" when the measured distance error is within 1% of the ground truth distance. While the conventional simple accumulation can detect large



Fig. 10. (a) Correlation between MP and NP versus the possibility of the two pixels watching the same object. The correlation is derived from PL and FL. (b) Simulation of 200-m range measurement comparing simple accumulation and SAT. We plot target size versus succession rate.

 TABLE I

 General Performance Comparison of Distance Quantizers

	TDC Time-to-Digital- Converter	ADC Analog-to-Digital- Converter	TDC/ADC Hybrid
Area	٢	8	•
Time Resolution	٢	8	\odot
Enable SAT?	8	\odot	٢

targets (>40 pixel²), it is challenging to detect small targets since non-target objects are also accumulated. On the other hand, with SAT, such non-target objects are efficiently filtered prior to accumulation and enables he detection of $4\times$ smaller targets. Therefore, we conclude that SAT has a $4\times$ higher effective image resolution compared to prior techniques. Note that if non-target objects are not generated, the difference between simple and SAT will be small. In this experiment, we aim to replicate an urban environment where multiple objects can exist within the accumulation window (as in Fig. 4), which is a challenging task for the simple accumulation technique.

IV. LIDAR CIRCUIT ARCHITECTURE

A. Conventional LiDAR Circuit Architecture Issues

In this section, we will discuss the LiDAR circuit architecture (Table I). In conventional LiDARs [4], [5], the TDC circuit has been frequently utilized as a distance quantizer. The largest merit upon using TDC is that extremely fast time resolution (<100 ps) can be achieved with very small area. Even TDCs capable of multiple measurements have been presented [23]. However, TDCs cannot acquire amplitude information, since it only measures the ToF when the input exceeds a certain value. Therefore, SAT cannot be utilized and LiDAR SBR will be limited. On the other hand, LiDARs utilizing ADCs have been presented [6], which can make the use of SAT and realize LR high-image-quality LiDARs. Nevertheless, the ADC circuitry has a slow sampling rate and large silicon area when compared to TDCs.

For ADAS LiDAR systems, sub-centimeter precision (rms distance error) is required at short distances for reliable parking assists and curb detections, and the required time resolution to achieve sub-centimeter error is approximately 100 ps (10 GS/s). For an example, a state-of-the-art 8-bit 16 GS/s ADC in 28-nm standard CMOS occupies an area of 0.6 mm² [25]. The 20 channels of such ADCs would consume an unrealistic silicon area of 12 mm² and will dominate the cost of LiDAR SoCs.

B. Proposed Hybrid Architecture

To realize a LiDAR SoC with low area and high precision for short distances, we propose the ADC/TDC hybrid architecture shown in Fig. 11. Both TDC and ADC are distance quantizers by making the use of the relaxed ToF error requirements. Generally, LiDAR requires precise DMs for short distances. However, the precision requirements are relaxed for longer DMs. This is shown in Fig. 12, where the target ToF measurement error is relaxed for longer measurement distances.

For short-range (SR) measurements under 20 m, the 12-bit, 40-ps time-resolution TDC can easily achieve sub-centimeter precision. Moreover, the proposed hybrid architecture significantly relaxes the ADC sampling rate to 400 MS/s since distance precision is greatly relaxed for LR measurements (20–200 m). Due to the hybrid architecture, the relaxed ADC sampling rate allows us to design ADCs with significantly reduced area. We would like to emphasize that ADC area reduction makes up for implementing the SR and LR circuitries, respectively, since 10 GS/s ADCs are magnitude larger than 400 MS/s ADCs.

The LiDAR SoC block diagram incorporating the TDC/ADC hybrid architecture is shown in Fig. 11. For short distances (<20 m), TDC operates without SAT; the reflected laser light is strong and sufficient LiDAR SBR can be achieved without accumulation. The TDC circuitry implements sunlight tolerance by setting a finite threshold (V_{th}) upon triggering its operation [4]. On the other hand, for LR measurements (20-200m), SAT is utilized to enhance the LiDAR SBR without degrading the image quality. Since the TDC triggering threshold is set high enough so that it will not be triggered by background photons, the TDC output can be relied on. Therefore, when determining the pixel's ToF results, TDC results are utilized if TDC results exist [24]. If not, the ToF is derived through the ADC data processing pipeline, which is explained in the following. First, if the measurement utilizes temporal accumulation, the ADC output is averaged for N times. Then, the averaged ADC output will be processed by the SAT algorithm and spatial accumulation is executed. Next, peak



Fig. 11. LiDAR SoC block diagram.



Fig. 12. Concept of the hybrid architecture.

detection is done where the highest ADC output is simply selected, and the ToF result is derived with interpolations.

Upon realizing the hybrid architecture, we designed an optical system where the incoming light is split and injected to two types of SiPMs, SR-SiPM and LR-SiPM, respectively, and these two SiPM are optimized to improve the LiDAR performance. Since the laser light reflecting from SR targets is strong, the SiPM output may saturate and worsen measurement precisions. To prevent such issues, the number of SPAD cells in SR-SiPM is increased substantially. To the contrary, our LR-SiPM is structured to maximize the quantum efficiency, which is the most important ability for LR measurements. To minimize the optical loss, the optical system is designed to realize the unsymmetrical photon distribution with LR-SiPM and SR-SiPM; the photons are concentrated to the LR-SiPM which has significantly strict SBR.

The drawback of the hybrid architecture is the offset generated between the SR and LR path, which will affect the monotonicity and linearity of the LiDAR. This result mainly because of differed print board patterning and SiPM timing constants, which is difficult to eliminate. Therefore, we compensate this problem by utilizing replica LR and SR measurement blocks, respectively. A pilot signal, generated by replica SiPMs (not shown), is input to the LR and SR block simultaneously, to generate a measurement result with a known ToF. Thus, by comparing the ToF results, the offset is easily derived and is removed digitally during the LiDAR operation. Since timing offset due to circuit mismatches were small, we do not calibrate inter-channel offsets in this design.

V. CIRCUIT IMPLEMENTATION

A. Long-Range TIA Designs

Fig. 13 shows the schematic of the LR analog frontend (AFE) path, illustrating mostly the trans-impedance amplifier (TIA). The TIA is mainly composed of two stages, where the first stage is the transimpedance stage and the second stage transforms the signal to single-to-differential and I-to-V, respectively. An additional buffer amplifier drives the ADC input and also transfers the power domain 1.8–0.9 V.

To achieve the best LiDAR performance, a wide signal bandwidth (BW) of 100 MHz is required. To achieve 100-MHz BW while driving a large printed circuit board loading capacitance (30-50 pF), the transimpedance stage was realized by regulated common-gate amplifier [21] to enable low input impedance of 30 Ω . The regulated amplifier was designed with a two-stage opamp to achieve high gain, and its stability was carefully designed. While SiPMs' output currents vary from 100 μ A to few milliamperes, the TIA may saturate if the dc current (I_{DC}) is insufficient. In our design, the dc current (I_{DC}) is configurable for ± 10 dB; the SoC can cope with various SiPMs. The two-stage TIA adds flexibility to the system but comes with a cost of additional power and area overhead. While the regulated amplifier dominates the TIA noise (the TIA input referred noise was 1.2 μ A_{rms}), this noise is small compared to the SiPM single-photon current output (8 μ A) and has small effect to the LiDAR performance. For an example, even if the TIA input referred noise was to be doubled to 2.4 μ A_{rms}, system simulation showed that the LiDAR's success rate or precision will not be affected.

B. Residue-Quantized Noise-Shaping SAR ADC

When realizing an 8-bit ADC in deeply scaled CMOS, it is likely that SAR ADC achieves the best performance due to its digital friendly nature [26]. Generally, in an SAR ADC,



Fig. 14. Concept and block diagram of RQNS SAR ADC.

the C-digital-to-analog-converter (C-DAC) area is dominating since it enlarges exponentially with the increase with the ADC bit, which limits the operation frequency. Hence, to enhance the sampling rate up to our target, 400 MS/s, area-consuming time-interleaving technique will be required. Therefore, SAR ADC with the noise-shaping (NS) technique [27] is used for our LiDAR SoC, to enhance the conversion accuracy per cycle by NS. Since the quantization noise is shaped, the C-DAC resolution and SA cycles required to achieve a certain signal-toquantization ratio (SQNR) is relaxed, leading to smaller area.

On the top of that a 2nd-order residue-quantizing NS (RQNS) technique is proposed to further enhance SQNR and area. In the conventional NS-SAR ADC, to process the analog residue, area-consuming sample and hold (S/H) and switched capacitor (SC) circuits were required to achieve the optimum noise transfer function (NTF). Therefore, the merits were limited to SQNR enhancement and not area reduction. The proposed RQNS shifts the residue processing to the digital domain, where the signal processing has a low power and area cost; the amplification can be conducted by bit shifts and sampling circuits by only few flip flops. This enables the NS-order enhancement with minimum area penalty.

Fig. 14 shows the concept and block diagram of the RQNS SAR ADC. The residue quantizer is composed of 3-bit SAR ADC samples and quantizes the residue generated at the main 5-bit SAR ADC prior to the next conversion in a pipelined fashion. Therefore, the speed penalty due to residue quantization is small. The quantized residue is sent to the digital-domain residue feedback circuit, where the residue is stored and amplified to achieve the optimum 2nd-order NTF. The C-DAC schematic with the residue feedback mechanism is shown in Fig. 14. It consists of two parts: the main C-DAC where it conducts the SAR operation and the residue C-DAC which handles the quantized residue for the NS operation. In this design, the unit capacitors receiving $D_{\text{res}}[z-1]$ are sized $2 \times$ larger to prevent overflow, since the 3-bit results are bit shifted to the left upon input. The comparator offset between the main and the residue-quantizing SAR ADC can cause performance degradation. While not shown in Fig. 14, an additional offset canceling DAC is connected to compensate the offsets to the main and residue-quantizing SAR ADC, respectively. A bang-bang calibration is conducted upon SoC startup, where DAC codes to cancel the offset is acquired.

In ToF measurements, ADC sampling rate is crucial for ToF precision rather than the input signal BW; therefore, oversampling is acceptable. In our LiDAR system, there was no effect to the ToF performance up to oversampling ratio (OSR) = 2, but some precision degradation was confirmed above OSR = 4. Therefore, OSR = 2 was chosen. For systems compatible with higher OSRs, due to the nature of digital-domain residue processing, RQNS ADCs can easily utilize 3rd-order or higher NS to achieve higher SQNR without significant circuit overheads. In addition, while most NS-SAR ADCs [27]-[30] utilize four-input comparators to feedback the residue,



Fig. 15. Measurement results of the SAR ADC. (a) Spectrogram of the ADC output with 9.8-MHz sinusoidal input. (b) Performance summary of the measured SAR ADC. (c) Power versus area benchmark against ADCs presented at past ISSCC (data based on [31]).

four-input comparator offset is easily modulated by power supply and common-mode variations; therefore, the ADC performs with low common-mode noise rejection ratio (CMRR) and power supply noise rejection (PSR). This cannot be overlooked since automotive applications demand high reliability to circuits. On the other hand, our RQNS ADC feedback the residue via C-DAC and allows us to use high-reliability two-input comparators; hence, the ADC sustains high CMRR and PSR.

The measurement results of the ADC alone are demonstrated in Fig. 15. The 2nd-order NS is accomplished due to the RQNS; NS of 40 dB/dec is confirmed at the spectrum [Fig. 15(a)] and SNDR = 37.7 dB is achieved at OSR = 2. The measurement results are confirmed with all 20-ch ADCs operating simultaneously with large power supply variations. However, there is almost no SNDR degradation compared with measurement conducted with only 1-ch ADC. The ADC achieves the smallest area among previously reported ADCs at ISSCC with SNDR > 35 dB and BW 50–400 MHz [Fig. 15(b) and (c)]. Note that the ADC area is described without decoupling capacitors. When included, the ADC area will increase 20%.

C. Short-Range Analog Front End

Fig. 16 shows the block diagram of the AFE for SR-DM. The AFE consists of TIA, constant-fraction



Fig. 16. AFE for SR-DM (top). Principle of CFD (bottom).



Fig. 17. Measured SR-DM non-linearity against excited SiPM cells.

discriminator (CFD), and TDC circuits. The TIA adopts the same architecture as the LR, which receives the current signal from SR-SiPM with 100-MHz BW and converts to a voltage signal for the successive signal processing in the TDC. The TDC is simply triggered when the TIA output reaches a certain threshold, set to neglect sunlight excitations. The comparator output (DM_Stop) triggers the TDC to acquire high-precision ToF measurement results. However, non-linearity remains a serious problem in TDC-based architectures. As shown in Fig. 16 (bottom left), if the output current (excited cell number) of the SiPM changes with the target reflectivity or distance, the triggered timing also alters due to the constant threshold value, resulting in a large non-linearity. We tackle this issue by utilizing a CFD circuit as in [22]. The CFD compares the delayed and non-delayed input signals and equivalently detects the zero-crossing timing of the differentiated input signal; thus, a time-invariant TDC trigger signal can be generated [as illustrated in Fig. 16 (bottom right)]. The measured SR-DM non-linearity against the excited SiPM cells is plotted in Fig. 17. This graph proves that CFD successfully cancels the rise time dependence, resulting in $a < \pm 1$ cm non-linearity.

Fig. 18 shows the block diagram of the 40-ps LSB 20-ch TDC for SR-DM. The TDC utilizes an architecture similar to [4], except that all-digital (AD) phase-locked loop (PLL) is used and not analog PLL, to further reduce chip area. An eight-phase ring digitally controlled oscillator (DCO) has a 3-bit phase information, which is phase locked by an AD PLL. The integer phase information of the DCO is detected by a 9-bit binary counter, resulting in a total measurable range of 12 bits (0–20 m). The DCO and the counter are shared among the 20-ch D-type flip-flop (DFF) latches, constructing the 20-ch TDC. Fig. 19 shows the measured result of SR-DM error, measured by injecting SiPM-simulated signal with a

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Fig. 19. Measured SR-DM precision.



Fig. 20. Chip photograph of the LiDAR SoC fabricated in 28-nm CMOS.

known ToF to the LiDAR SoC. Such electrical simulated measurements were mandatory in order to efficiently conduct thousands of SR-DM. The measured result confirms that the SR-DM block achieves 1-cm precision at range of <10 m and 0.1% precision at range of 10–20 m.

VI. MEASUREMENT RESULTS

The proposed TDC/ADC hybrid LiDAR SoC was fabricated in 28-nm CMOS (Fig. 20). The LiDAR system was developed by integrating optical systems, SiPM, and SoC (Fig. 21). To accomplish quantitative comparisons between the state-ofthe-art works, we will build an outdoor DM system based on [4], illustrated in Fig. 22. We prepare a moveable target which is covered with a material having a 10% reflectivity. At 200-m distance, the target was 14 pixel² in size and the SAT accumulation window was set to 27 pixel² to fully cover the target and maximize SBR. During measurement, the downpour



Fig. 21. Our developed LiDAR system.



Fig. 22. Outdoor measurement setup.

of sunlight was 100 klx, and when the luxmeter was hold up to the LiDAR input, it showed 70 klx, which is very similar to the condition in [4]. While the horizontal resolution is flexible in our LiDAR system (1920–240), we set this to 240 in order to enclose to the condition in [4]. This allows us to utilize temporal averaging, where each pixel was measured and averaged for eight times, respectively. The LiDAR obtains the entire image with 10 frames/s, and the average laser power was 50 mW. A calibration was carried out beforehand to eliminate offsets induced by mismatches.

We measured the target distance starting from 20 m and with a 40-m interval (20, 60, 100, 140, 180, 200, and 220 m) with SAT enabled. Fig. 23(a) shows the ground truth distance versus measured distance (averaged $1000 \times$) to evaluate static errors. The distance error is only 0.1% at 200 m (20-cm error). Fig. 23(b) shows the measurement distance against success rates. Up to 180 m, the success rate is 100%, and at 200 m, 92.7% success rate is accomplished. Since our design goal was accomplishing 90% success at 200 m, the results satisfy our design targets. For reference, the success rate was dropped to 60% at 220-m distance. Fig. 23(c) shows the measurement's dynamic errors (standard deviation) or repeatability errors, and note that this is computed only from the successful measurements. The dynamic errors at 200 m were 250 mm, which is 0.125% of the measured distance. Throughout the range of 20-200 m, the dynamic errors stay within 0.125% of the distance. While the quantum efficiency of the LR-SiPM has not been directly measured, we estimate that it is around 5% comparing Fig. 16 results and system simulation results.



Fig. 23. Outdoor measured performance of the LiDAR system. (a) Actual ground truth distance versus measured distance by LiDAR. (b) Distance versus success rate, where we define the success as measurement with $\pm 1\%$ error. (c) Distance versus dynamic error.



Fig. 24. Range image acquired in urban situation. (a) Range image with SAT. (b) Range image without SAT (no accumulation). (c) Range image without SAT (simple accumulation).

The range images captured by the LiDAR with SAT, without accumulation, and with simple accumulations are shown in Fig. 24(a)–(c), respectively. Note that this image is captured with 1920 × 96 resolution and 10 frames/s with 20-mW average laser power. The laser power is in a range where it would pass class-1 eye safety standards with a significant margin. Fig. 24(b) shows the distance image where it was captured without using any accumulation techniques. As we had discussed in Section II, high image quality can be achieved, but the LiDAR SBR is low; it fails to recognize the pedestrian at LR. Moreover, it is interesting that the LiDAR fails to recognize the road as well, which is an object that has low reflectivity. Fig. 24(c) shows a distance image acquired by utilizing "simple" accumulation with a 3×9 window. Since the



Fig. 25. 3-D point-cloud image taken with our LiDAR system.

LiDAR SBR is improved by accumulation, it succeeds upon acquiring the road. However, a strong "Blur" effect is induced, and the image quality is poor and note that it fails to acquire small objects such as the pedestrian. Finally, the distance image acquired by utilizing SAT is shown in Fig. 24(a). Since SAT conducts a simple binary object classification upon accumulation, the LiDAR SBR is enhanced significantly while sustaining high image quality. While it is challenging to detect small objects with simple accumulation, SAT can recognize the pedestrian, thus suitable for self-driving applications.

Fig. 25 shows a snapshot of a daytime 3-D point-cloud image taken with our proposed LiDAR system at a reallife environment. This is acquired by enabling SAT and with 10 frames/s. For better understanding, the objects included in the image were surrounded by red rectangles and tagged by the authors. In ADAS driving tasks, the distance images are passed on to cognitive image processors, which will recognize the surrounding objects using data with a fusion with camera and millimeter-wave radar data.

Table II shows the LiDAR performance comparison. The proposed LiDAR using the proposed hybrid SoC and SAT achieves $2 \times$ longer DM and $4 \times$ higher effective pixel reso-

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 TABLE II

 Performance Comparison With State-of-the-Art LiDAR Socs

	This Work	Niclass JSSC 2014[4]	Akita VLSI 2017[7]
Technology	28nm	180nm HV	180nm
SPADs	Off-chip	On-chip	On-chip
Optical System	Mechanical Mirror	Mechanical mirror	MEMS mirror
Pixel-Resolution	240x96	202x96	N.A.
Effective Pixel-Resolution w/ accumulation	4x	1x	N.A.
Laser Wavelength [nm]	905	870	870
Laser average power [mW]	50	21	N.A.
Laser repetition rate [MHz]	0.03	0.133	N.A.
FPS	10	10	N.A.
Target Reflectivity	10%	9%	10%
Background light [klux]	70	70	75
Distance range [m]	200	100	20
1 sigma error @max distance	0.125%	0.14%	0.5%
SoC power consumption [W]	4	0.53	N.A.

lution than conventional designs with almost equivalent FPS. Considering the laser photon's distance divergence and if the same laser power was used in [4], our proposed LiDAR can achieve $1.4 \times$ longer range DM thanks to the ADC-based quantization and SAT.

VII. CONCLUSION

A TDC/ADC hybrid LiDAR SoC to realize reliable selfdriving systems was presented. The SAT-based quantization and ADC-based quantization are the key technologies upon achieving 200-m range imaging with a high image quality, which was untrodden with conventional LiDARs. The "smart" accumulation was realized by utilizing simple object recognition with small circuit overhead; compared to conventional "simple" accumulations, the LiDAR range and precision are enhanced significantly without degrading the pixel resolution. Moreover, a TDC/ADC hybrid architecture was proposed to achieve a wide-distance-range LiDAR with a small silicon area and sub-centimeter precision at short distances. To further downscale the ADC cost, an RQNS SAR ADC was proposed.

The prototype LiDAR SoC was fabricated in the 28-nm CMOS technology. The LiDAR measured with 240 \times 96 pixels at 10 frames/s achieved a measurement range of 200 m even with 70-klx direct sunlight: the measurement range is 2 \times longer than conventional designs. Furthermore, our LiDAR achieved 4 \times higher effective pixel resolution compared to conventional designs using simple accumulation.

REFERENCES

- SAE J3016. Taxonomy and Definitions for Terms Related to Driving Automation Systems for on-Road Motor Vehicles. Accessed: Aug. 15, 2018. [Online]. Available: https://www.sae.org/standards/ content/j3016_201806/
- [2] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.
- [3] F. Liu, C. Shen, and G. Lin, "Deep convolutional neural fields for depth estimation from a single image," in *Proc. IEEE Comput. Vis. Pattern Recognit. (CVPR)*, Jun. 2015, pp. 5162–5170.

- [4] C. Niclass, M. Soga, H. Matsubara, M. Ogawa, and M. Kagami, "A 0.18-μm CMOS SoC for a 100-m-range 10-frame/s 200×96-pixel time-of-flight depth sensor," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 315–330, Jan. 2014.
- [5] C. Niclass, M. Soga, H. Matsubara, S. Kato, and M. Kagami, "A 100 m-range 10-frame/s 340×96-pixel time-of-flight depth sensor in 0.18μm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 559–572, Feb. 2013.
- [6] Velodyne. Velodyne's Hdl-64E: A High Definition Lidar Sensor For 3-D Applications. Accessed: Aug. 15, 2018. [Online]. Available: http:// velodynelidar.com/docs/papers/HDL%20white%20paper_OCT2007_ web.pdf
- [7] H. Akita, I. Takai, K. Azuma, T. Hata, and N. Ozaki, "An imager using 2-D single-photon avalanche diode array in 0.18-μm CMOS for automotive LIDAR application," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2017, pp. 290–291.
- [8] C. Niclass *et al.*, "Design and characterization of a 256×64-pixel singlephoton imager in CMOS for a MEMS-based laser scanning time-offlight sensor," *Opt. Express*, vol. 20, no. 11, pp. 11863–11881, 2012.
- [9] C. V. Poulton et al., "Coherent solid-state LIDAR with silicon photonic optical phased arrays," Opt. Lett., vol. 42, no. 20, pp. 4091–4094, 2017.
- [10] S. W. Chung, H. Abediasl, and H. Hashemi, "A 1024-element scalable optical phased array in 0.18 μm SOI CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 262–263.
- [11] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128×128 single-photon imager with on-chip column-level 10 b timeto-digital converter array capable of 97 ps resolution," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2977–2989, Dec. 2008.
- [12] S. Koyama *et al.*, "A 220 m range direct timeof flight 688×384 CMOS image sensor with sub photon signal extractionpixels using vertical avalanche photo diodes and 6 kHz light pulse counters," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018.
- [13] S. Lindner, C. Zhang, I. Antolovic, M. Wolf, and E. Charbon, "A 252×144 SPAD pixel FLASH LiDAR with 1728 dual-clock 48.8 ps TDCs, integrated histogramming and 14.9-to-1 compression in 180 nm CMOS technology," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018.
- [14] M. Perenzoni, D. Perenzoni, and D. Stoppa, "A 64 × 64-pixels digital silicon photomultiplier direct TOF sensor with 100-MPhotons/s/pixel background rejection and imaging/altimeter mode with 0.14% precision up To 6 km for spacecraft navigation and landing," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 151–160, Jan. 2016.
- [15] K. Yoshioka *et al.*, "A 20ch TDC/ADC hybrid SoC for 240×96-pixel 10%-reflection <0.125%-precision 200m-range imaging LiDAR with smart accumulation technique," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 92–93.
- [16] S. Kawahito, I. A. Halin, T. Ushinaga, T. Sawada, M. Homma, and Y. Maeda, "A CMOS time-of-flight range image sensor with gates-onfield-oxide structure," *IEEE Sensors J.*, vol. 7, no. 12, pp. 1578–1586, Dec. 2007.
- [17] C. S. Bamji *et al.*, "A 0.13 μ m CMOS system-on-chip for a 512 × 424 time-of-flight image sensor with multi-frequency photo-demodulation up to 130 MHz and 2 GS/s ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 303–319, Jan. 2015.
- [18] C. S. Bamji *et al.*, "IMpixel 65 nm BSI 320 MHz demodulated TOF image sensor with 3 μm global shutter pixels and analog binning," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 94–95.
- [19] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Appl. Opt.*, vol. 35, no. 12, pp. 1956–1976, 1996.
- [20] P. Buzhan et al., "Silicon photomultiplier and its possible applications," Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip., vol. 504, nos. 1–3, pp. 48–52, 2003.
- [21] M. de Medeiros Silva and L. B. Oliveira, "Regulated common-gate transimpedance amplifier designed to operate with a silicon photomultiplier at the input," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 725–735, Mar. 2014.
- [22] D. Binkley, "Performance of non-delay-line constant-fraction discriminator timing circuits," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 4, pp. 1169–1175, Aug. 1994.
- [23] N. A. W. Dutton *et al.*, "A time-correlated single-photon-counting sensor with 14 GS/S histogramming time-to-digital converter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
- [24] K. Tanabe, H. Kubota, A. Sai, and N. Matsumoto, "Data selection and de-noising based on reliability for long-range and high-pixel resolution LiDAR," in *Proc. IEEE COOL CHIPS*, Apr. 2018, pp. 1–3.

front-end with programmable gain control and analog peaking in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 58–59.

- [26] K. Yoshioka et al., "A 0.7 V 12 b 160 MS/s 12.8 fJ/conv-step pipelined-SAR ADC in 28 nm CMOS with digital amplifier technique," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 478–479.
- [27] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.
- [28] C.-C. Liu and M.-C. Huan, "A 0.46 mW 5 MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 466–467.
- [29] W. Guo and N. Sun, "A 12 b-ENOB 61 μ W noise-shaping SAR ADC with a passive integrator," in *Proc. IEEE ESSCIRC*, Sep. 2016, pp. 405–408.
- [30] Y.-S. Shu, L.-T. Kuo, and T.-Y. Lo, "An oversampling SAR ADC With DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, Dec. 2016.
- [31] B. Murmann. ADC Performance Survey 1997– 2017. Accessed: Aug. 15, 2018. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html



Kentaro Yoshioka received the B.S. and M.S. degrees from Keio University, Tokyo, Japan.

Since 2017, he has been a Visiting Scholar with Stanford University, Stanford, CA, USA, where he has been exploring efficient machine learning hardware. He is currently with Toshiba Corporation, Kawasaki, Japan.

Mr. Yoshioka was a recipient of the ASP-DAC 2013 Special Feature Award and the A-SSCC 2012 Best Design Award.



Hiroshi Kubota received the B.S. and M.S. degrees from University of Tokyo, Tokyo, Japan. He is currently with Toshiba Corporation, Kawasaki, Japan.

Tomonori Fukushima, photograph and biography not available at the time of publication.



Satoshi Kondo received the B.E. degree in electrical engineering from the Gunma National College of Technology, Gunma, Japan, in 2012, and the M.E. degree in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2014.

In 2014, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. His current research interests include mixed-signal circuit design and digitally assisted frequency synthesizers.



Tuan Thanh Ta (M'14) was born in Hanoi, Vietnam, in 1983. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 2008, 2010, and 2013, respectively.

He is currently a Researcher with Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. His current research interests include devices for sensing techniques and low-power, high-speed wireless systems, especially in RF signal processing integrated circuits.

Dr. Ta is a member of IEICE, Japan.



Hidenori Okuni received the B.E. and M.E. degrees in communications engineering from Tohoku University, Sendai, Japan, in 2002 and 2004, respectively.

Since 2004, he has been with the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. His current research interests include low-power wireless communication systems.

Kaori Watanabe received the B.S. and M.S. degrees from Hokkaido University, Sapporo, Japan.

From 2016 to 2018, she was with the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where she focused on phase-locked loop (PLL) and LNA circuits.

Masatoshi Hirono, photograph and biography not available at the time of publication.



Yoshinari Ojima is currently a System LSI Development Engineer with Toshiba Electronic Device & Storage Corporation, Kawasaki, Japan.

Katsuyuki Kimura received the B.S. and M.S. degrees from Keio University, Tokyo, Japan.

He was with Toshiba Corporation, Kawasaki, Japan, where he was involved in the research and development of various image processing large-scale integration (LSI) for over 15 years. He is currently an In Charge of research and development of image recognition processors and electronic devices for LiDAR with Toshiba Electronic Devices & Storage Corporation, Kawasaki, Japan.



Sohichiroh Hosoda received the B.E. and M.E. degrees from Waseda University, Tokyo, Japan. Since 2005, he has been with Toshiba Corporation, Kawasaki, Japan, where he engaged in developing in-system programming (ISP) circuits and automotive circuits.



Yutaka Ota received the B.S. degree from Tokyo University, Tokyo, Japan. He is currently with Toshiba Corporation, Kawasaki, Japan.

Tomohiro Koizumi, photograph and biography not available at the time of publication.

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Naoyuki Kawabe received the B.E. and M.E. degrees in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1995 and 1997, respectively.

In 1997, he joined Toshiba Corporation, Kawasaki, Japan, where he was engaged in the research and development of system-on-chip (SoC) design methodology and CAD systems, especially for low power. In 2018, he joined Toshiba Memory Corporation, Yokohama, Japan. Since 2007, he has been involved in SoC design.

Yasuhiro Ishii, photograph and biography not available at the time of publication.

Yoichiro Iwagami, photograph and biography not available at the time of publication.

Seitaro Yagi, photograph and biography not available at the time of publication.

Isao Fujisawa, photograph and biography not available at the time of publication.



Nobuo Kano received the B.S., M.S., and Ph.D. degrees from Tokyo Denki University, Tokyo, Japan, in 1991, 1993, and 1997, respectively.

He is currently with the Mixed Signal IC Division, Toshiba Electronic Devices & Storage Corporation, Kawasaki, Japan. He is involved in the development of analog CMOS integrated circuits.



Tomohiko Sugimoto received the M.S. degree from Kobe University, Kobe, Japan.

He is currently an Engineer with Toshiba Electronic Device & Storage Corporation, Kawasaki, Japan. His current research interests include data converters.



Daisuke Kurose (M'12) received the B.S. degree in electronics engineering from Fukuoka University, Fukuoka, Japan, in 1999, and the M.S. degree in information science and electrical engineering from Kyushu University, Fukuoka, in 2001.

In 2001, he joined Toshiba Corporation, Kanagawa, Japan, where he is involved in the design of data converters.



Yumi Higashi received the B.S. and M.S. degrees from the Kyushu Institute of Technology, Kitakyushu, Japan, in 1996 and 1998, respectively. She has been with Toshiba Memory Corporation, Yokohama, Japan, where she has been engaged in the development of analog CMOS integrated circuits.

Tetsuya Nakamura received the B.S. and M.S. degrees from Kyushu University, Fukuoka, Japan. He is currently with Toshiba Corporation, Kawasaki, Japan.

Yoshikazu Nagashima received the B.S. and M.S. degrees from the Nagoya Institute of Technology, Nagoya, Japan.

From 1993 to 2016, he was with Toshiba Corporation, Kawasaki, Japan. He is currently with Toshiba Memory Corporation, Yokohama, Japan. His current research interests include high-speed serial interface system design.



Hirotomo Ishii received the B.E. and M.E. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1995 and 1997, respectively.

In 1997, he joined Toshiba Corporation, Kawasaki, Japan. He is currently with Toshiba Electronic Devices & Storage Corporation, Kawasaki, where he has been engaged in the development of high-performance data converters and mixed signal ICs.



Akihide Sai received the B.E. and M.E. degrees from Waseda University, Tokyo, Japan, in 2002 and 2004, respectively.

In 2004, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. Since 2005, he has been engaged in the research and development of analog/ mixed-signal circuits for wireless communications. He is currently a Research Scientist with Toshiba Corporation and involved in the development of lower power transceivers and digital/analog

phase-locked loops (PLLs). His current research interests include digital-assist techniques for high-performance mixed-signal systems.



Naoya Waki received the B.E. and M.E. degrees in electrical engineering from the Tokyo University of Science, Tokyo, Japan, in 2006 and 2008, respectively.

Since 2008, he has been with Toshiba Corporation, Kawasaki, Japan. His current research interests include analog integrated circuit and analog-todigital converter.

Mr. Waki received the 2006 IEEJ Analog VLSI Workshop Young Researcher IEEE CAS Japan Chapter Sponsorship Award of the 2006 IEEJ International Analog VLSI Workshop.



Nobu Matsumoto received the M.E. degree from Waseda University, Tokyo, Japan.

In 1983, he joined Toshiba Corporation, Kawasaki, Japan. Since 1984, he has been engaged in the research and development of media-embedded processors, software-development tools/operating systems, electronic system-level (ESL) design methodology, and novel sensor technology.