A 1 GS/s 10b 18.9 mW Time-Interleaved SAR ADC With Background Timing Skew Calibration

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***Abstract*—This paper presents a time-interleaved (TI) SAR ADC which enables background timing skew calibration without a separate timing reference channel and enhances the conversion speed of each SAR channel. The proposed ADC incorporates a flash ADC operating at the full sampling rate of the TI ADC. The flash ADC output is multiplexed to resolve MSBs of the SAR channels. Because the full-speed flash ADC does not suffer from timing skew errors, the flash ADC output is also used as a timing reference to estimate the timing skew of the TI SAR ADCs. A prototype ADC is designed and fabricated in a 65 nm CMOS process. After background timing skew calibration, 51.4 dB SNDR, 59.1 dB SFDR, and ±1.0 LSB INL/DNL are achieved at 1 GS/s with a Nyquist rate input signal. The power consumption is 18.9 mW from a 1.0 V supply, which corresponds to 62.3 fJ/step FoM.**

***Index Terms*—ADC, analog-to-digital converter, background timing skew calibration, SAR ADC, subrange SAR ADC, successive approximation register ADC, time-interleaved ADC, timing skew calibration, timing skew.**

I. Introduction

ALTHOUGH device scaling has helped to increase the conversion rate of single-channel medium-to-high resolution ADCs, the improvement is still insufficient to meet the requirements of recent high-speed applications, such as high-speed digital oscilloscopes, optical communications, direct sampling receivers, and digitally equalized data links [1]–[4]. A time-interleaved (TI) ADC architecture can increase the effective conversion rate of an ADC by multiplexing several ADCs in parallel. The effective conversion rate of a TI ADC (f_s) can be expressed as $f_s = f_c \times N$, where f_c and N are the conversion rate of each channel and the number of the interleaved channels, respectively. The power efficiency is another benefit of TI ADCs. Generally, power consumption of an ADC grows much faster than proportional to the conversion rate of the ADC. However, in the time-interleaved structure, the effective conversion rate can be increased by N times at the cost of only N times power consumption plus the power increase in the clock distribution.

Ideally, the resolution of TI ADCs is the same as the resolution of the ADC in each channel. However, in reality, mismatches between the channels, such as offset mismatches, gain mismatches, and timing skews, introduce additional errors in TI ADCs and degrade the accuracy of the analog-to-digital conversion [5]. The error from offset mismatches is almost independent of input signal and does not change. The error from gain mismatches increase with input amplitude, but does not change with input frequency. One the other hand, timing skew causes errors that increase both input amplitude and input frequency [26]. Thus, for high-speed TI ADCs with a Nyquist-rate input signal, the timing skew can be a dominant error source.

Generally, timing skew calibrations are processed in two steps: timing skew measurement (or estimation) and error correction. Timing skew can be measured with a predetermined input signal such as a linear ramp [6] or a sine wave with known frequency [7]. This makes the measurement relatively easy and accurate. However, to apply such a specific input signal, the normal ADC operation must be interrupted for the calibration. Thus, these calibration techniques are limited to applications where ADCs are allowed a specific calibration period for a foreground calibration. Timing skew can also be measured with arbitrary inputs, which allows for background calibration. A correlation-based algorithm was developed in [8] to measure the timing skew in the background. It uses a dedicated timing reference ADC channel which does not suffer from timing skew as a reference for the time-interleaved channels. Reference [9] uses two additional ADC channels for a direct measurement of the timing skew error. One of them works as a timing reference for the TI channels and the other one is used to measure the derivative of the input signal. Both [8] and [9] present a new and robust algorithm, but the additional channels required for the calibration add power and area overhead. Another recent study in [10] demonstrated a background timing skew calibration without separate timing reference. However, this technique cannot support input signals close to or above Nyquist rate because the derivative of the input signal must be estimated from the input samples.

Once timing skew error is measured, the correction of timing skew error can be done in either the digital domain or the analog domain. Digital interpolation filters [6], fractional delay filters [11], and Taylor series approximations [12] are examples of digital filters for skew calibration. The cost in power consumption and area of the digital calibration block can be high, even in modern CMOS technology. In [2]–[4], programmable delay blocks are placed at the sampling clock to compensate the timing skew. This is the more practical and frequently used solution. However, the programmable delay blocks need to be designed carefully because the delay circuits tend to increase the noise and jitter of the clock signal.

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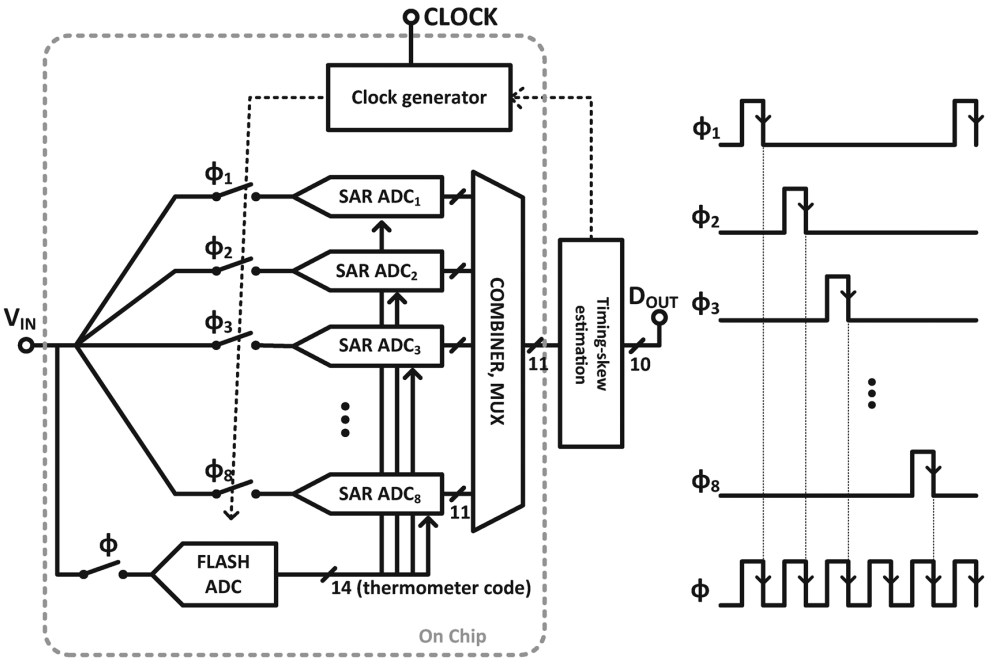


Fig. 1. Block diagram of the proposed TI SAR ADC.

This paper proposes a TI SAR ADC which allows a background timing skew calibration without a separate timing reference channel. The outline of this paper is as follows. Section II provides a block diagram of the chip and transistor level implementations of the prototype IC. A description of the proposed timing skew calibration and the behavioral simulation results are the subject of Section III, and in Section IV, the measured results are presented. Finally, conclusions are drawn in Section V.

II. Circuit Implementation

A. Block Diagram

Fig. 1 shows the block diagram of the time-interleaved SAR ADC and the timing waveform. The time-interleaved ADC is composed of a clock generator, a flash ADC, eight time-interleaved SAR ADCs, and digital circuits for bit combining and multiplexing. The flash ADC resolves MSBs (4 bit) at the full speed (ϕ) of the time-interleaved ADC and the flash ADC output is used as a coarse estimation of the SAR conversion [13]. Because it does not suffer from timing skew, the flash ADC output is also used as a timing reference. The SAR ADCs resolve LSBs (7 bit) at the divided clock speed $(\phi_1 \sim \phi_8)$ including 1 bit redundancy. The computation for timing skew estimation is performed off-chip. The timing skew estimator controls the programmable delay circuit in the sampling clock path to correct the timing skew error. The basic principle of the proposed background timing skew calibration is to align the sampling clock of SAR ADCs (ϕ_{X}) to the sampling clock of the flash ADC (ϕ). This calibration is explained in more detail with examples in Section III.

The resolution of the flash ADC in this work was chosen for a few practical reasons. The flash ADC resolution affects the calibration time. With higher resolution, flash ADC outputs provide more accurate timing information with lower quantization error. Thus, timing skew information can be extracted with fewer samples, as will be explained in Section III. However, the resolution of the flash ADC affects overall power consumption of the ADC. Power consumption of the flash ADC increases exponentially with its resolution. Although higher resolution flash ADC reduces the number of successive approximation cycles and the power consumption of the SAR ADC, the savings are marginal. With these consideration and behavioral simulation results, 4 bit flash resolution is chosen, and the remaining 7 bits including 1 bit redundancy are allocated in the SAR conversion.

One disadvantage of the proposed ADC structure is the increased input capacitance from two simultaneous active sampling paths. In this prototype, input capacitance of the flash ADC increases total input capacitance by 45%. However, the overhead can be mitigated by reducing unit capacitor size in the flash ADC since the noise requirement of the flash ADC is greatly relaxed by the over-range correction in the SAR ADC.

B. Clock Generation

Fig. 2 shows the block diagram of clock generation for the prototype. A low-voltage differential signal (LVDS) clock with $800\,\mathrm{mV_{pp,diff}}$ amplitude is provided externally and converted to a single-ended signal on-chip [14]. A global delay block shown in Fig. 2 corrects the average mismatch between the flash clock (ϕ) and the SAR clocks $(\phi_1 \sim \phi_8)$. Since they are located before the clock divider, the global delay block affects all SAR clocks equally and does not change the timing skew among SAR clocks. A clock divider, implemented with a chain of eight D-flip flops, is used to generate the divided clocks for the interleaved SAR channels $(\phi_1 \sim \phi_8)$ in Fig. 1. To minimize the systematic mismatches in the clock path, an H-tree structure is used to route clocks. The local delay block shown in Fig. 2 adjusts the timing of divided SAR clocks $(\phi_1 \sim \phi_8)$ separately to correct the timing skew among the SAR ADCs.

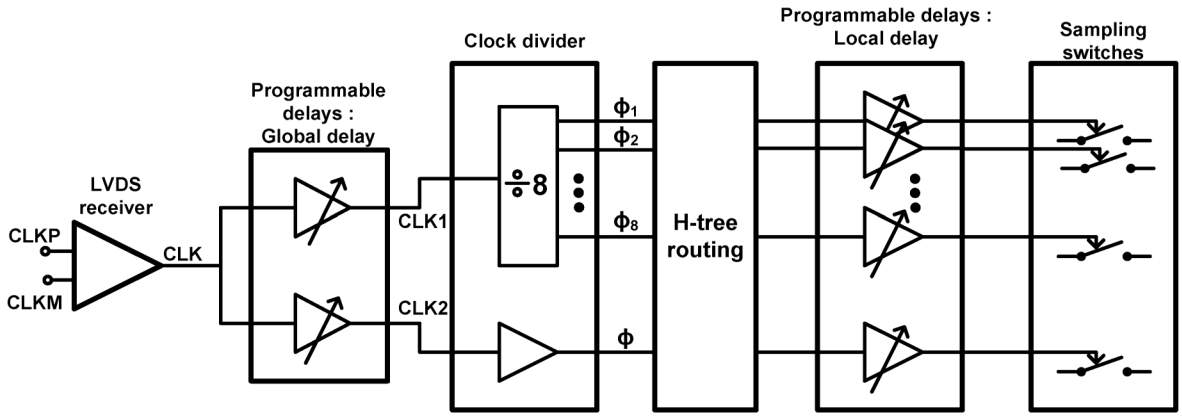


Fig. 2. Block diagram of clock generation.

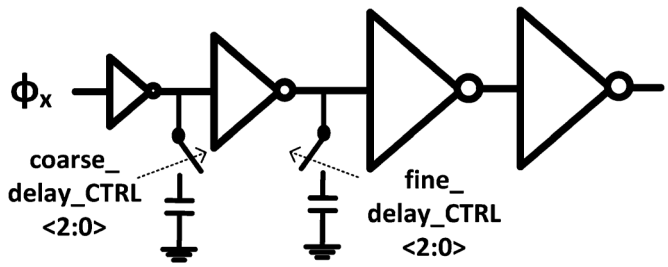


Fig. 3. Schematic of programmable delay block.

The schematic of the programmable delay block is shown in Fig. 3. It is composed of four inverters with different sizes. Two capacitor banks with switches are placed between the inverters to control the delay. Each capacitor bank has seven minimum-size MOS-capacitors which are controlled by a 3 bit binary code. Capacitors at the output of a small inverter control the coarse delay and capacitors at the output of a large inverter control the fine delay. The programmable delay block can increase clock jitter with a large capacitor load for a large delay. In the prototype, inverters for clock buffer are sized to achieve lower than 0.2 ps rms at the largest delay setting. The last two inverters are added to recover the sharpness of the transition edge. The coarse delay and fine delay are designed to have 2 ps and 0.8 ps delay steps, respectively. Timing skew correction range is approximately ± 10 ps which is determined based on the published works [2] and [3] and previous design experience in the same technology. With 0.8 ps fine calibration step, the residual timing skews after calibration are less than ± 0.4 ps with 0.23 ps RMS value. The targeted clock jitter and timing skews allows higher than 58 dB SNDR at Nyquist rate input for 10 bit 1 GS/s ADC.

C. Flash ADC

Fig. 4 shows the implementation of the flash ADC with the timing waveform. It is a 4 bit flash ADC with a capacitive DAC. Each comparator samples the input signal with a bottom plate switch on two capacitors with different sizes, which are then switched to the reference voltages $\mathrm{V_{REFP}}$ and $\mathrm{V_{REFN}}$ [15]. When the reference voltages settle, comparators are enabled. Although a single-ended version is shown for simplicity, a differential structure is implemented.

The bootstrap switches [16] are used for input tracking to minimize the variation of the on-resistance over a wide range of input voltages. The two sampling capacitors are sized to generate DAC voltages which are the thresholds of the flash ADC. A dynamic latch is used for the comparators in the flash ADC. Thanks to the redundancy between the flash and SAR ADCs, the offset requirements of the flash comparators are relaxed to the correction range which is $\pm 0.5\,\mathrm{LSB_{FLASH}}$ ($\pm 32\,\mathrm{LSB_{SAR}}$). The relaxed offset requirements can be met simply by proper sizing of the comparator, instead of having an offset cancellation circuit for each comparator.

The sampling flash ADC described in this section has several advantages over the conventional non-sampling flash ADC which compares the input directly with a reference voltage [15]. First, a rail-to-rail input range is enabled. Because most nonsampling flash comparators have limited common-mode range, a rail-to-rail input signal cannot be utilized. Second, it allows a true fully differential implementation. Although non-sampling flash comparators with two differential input pairs is topologically fully differential, when input or reference voltages are large, one of the differential pairs dominates resulting in effectively single-ended comparison. This causes errors when common-mode level is not stabilized and suffers from lower PSRR. Also, the lack of resistor ladders in the sampling flash comparator makes this flash ADC more power efficient. Finally, because it is a scaled version of a SAR ADC, the SAR and flash sampling instances are closely matched. This is especially important in this work, because the sampling clocks of SAR ADCs must be aligned as closely to the sampling clock of the flash ADC as possible to minimize the timing skew correction range.

D. SAR ADCs

Fig. 5 shows a 10 bit SAR ADC composed of 1024 unit capacitors, one comparator, and SAR logic. MSB DACs have 14 unary weighted capacitors each with a size of 64 and are controlled by the flash ADC output. LSB DACs are composed of binary weighted capacitors (size of 1 to 64) and controlled by a SAR logic block. One bit redundancy between the flash ADC and the SAR ADCs is added to correct the error from the flash ADC and to extract the timing skew information. A programmable delay block is placed in the sampling clock path

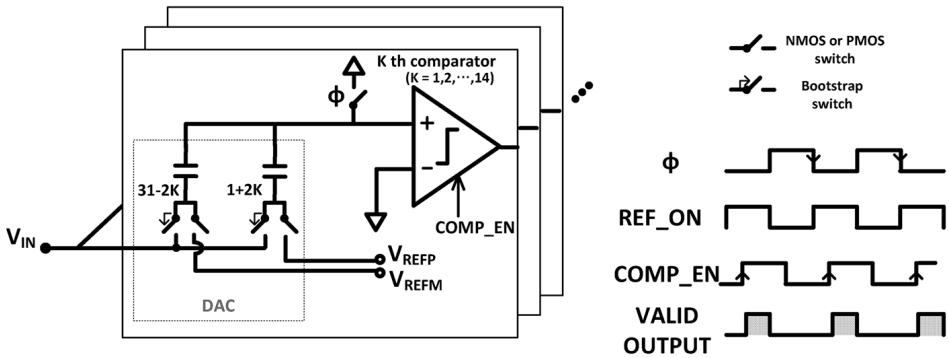


Fig. 4. Implementation of the 4 bit flash ADC (a single-ended version is shown for simplicity).

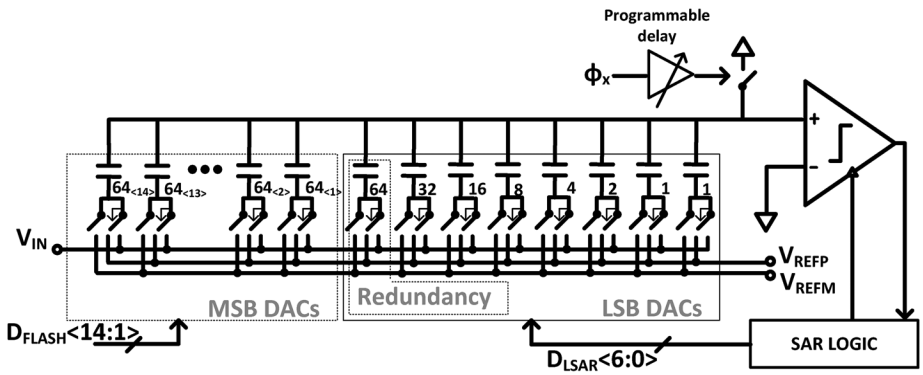


Fig. 5. Implementation of the 10 bit SAR ADC (a single-ended version is shown for simplicity).

to correct the timing skew. For the same reason as in the flash ADC, bootstrap switches are used for the input tracking, and NMOS or PMOS switches are used for the bottom plate sampling and the reference switches. To match bandwidth between the flash and SAR, bootstrap input tracking switches, sampling capacitors, and bottom plate sampling switches are scaled with the same ratio. The output of each channel $(\mathrm{D_{CHANNEL}})$ is the weighted sum of the flash ADC output $(\mathrm{D_{FLASH}})$ and the lower output bits of the SAR conversion $(\mathrm{D_{LSAR}})$, $\mathrm{D_{CHANNEL}} = 64 * \mathrm{D_{FLASH}} + \mathrm{D_{LSAR}}$. To avoid a high-frequency clock and to increase the SAR conversion speed, asynchronous SAR logic is implemented [17] with programmable delays.

When selecting a capacitor size, there are two main factors to consider: thermal (kT/C) noise and matching accuracy. The kT/C noise limits the minimum size of total capacitance to 100 fF on each side for a 10 bit ADC with $2\mathrm{V_{diff,pp}}$ input amplitude. This leads to a 0.1 fF unit capacitor for a 10 bit ADC, which is too small for 10 bit matching. According to published work using custom designed unit capacitors [18]–[21], 1 fF unit capacitors are a good compromise for 10 bit accuracy. The custom designed 1 fF unit capacitor used in the work is shown in Fig. 6. It is a combination of MIM and MOM structures [18], [22]. M3 and M5 are the two plates for the MIM structure. The insulating layer is the regular intermetal dielectric. The benefit of capacitor arrays with the MIM structure is that both the top and bottom plates form a large plane which shields top plate routing from bottom plate routing. Any parasitic capacitor between the top plate routing and bottom plate routing is added to unit capacitor. Thus, if the parasitic capacitor from routing is not equal to all unit capacitors, it causes a systematic capacitor mismatch. When a small unit capacitor is used, this benefit becomes more important, because parasitic capacitor from routing can be a significant portion of unit capacitor.

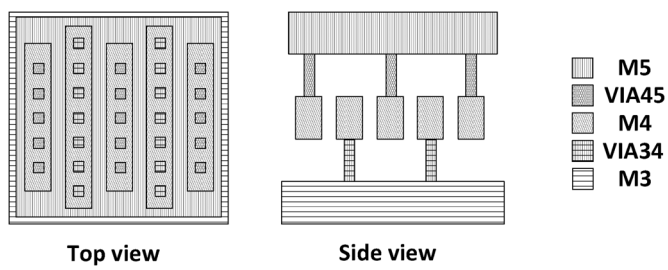


Fig. 6. Custom-designed unit capacitor.

However, the density of MIM capacitance without special dielectric layer is too low. To increase the density of the capacitor, interdigitated MOM structures are added in M4 and connected to M3 and M5. In the capacitor array, M5 is used as a bottom plate that is connected to the comparator input for smaller parasitic capacitance.

A dynamic latch with an offset control, shown in Fig. 7, is used for the SAR ADC comparator. An offset calibration block, which is a capacitor bank with switches, is added at both outputs of the comparator [23]. The offset calibration block has 31 switches and 31 capacitors controlled by the binary weighted 5 bit configuration bits. Although explicit capacitors are shown in Fig. 7, the parasitic capacitance of switches is used to control the offset finely. The parasitic unit capacitor is about 0.2 fF, and each unit capacitor adjusts comparator offset

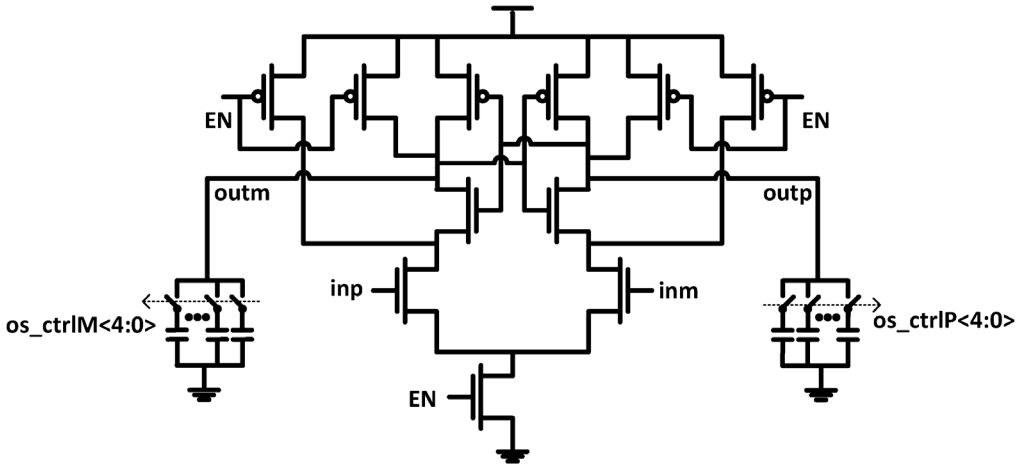


Fig. 7. Schematic of the SAR ADC comparator with offset calibration.

about 0.2 mV. Small capacitors also minimize the power and speed penalty caused by the additional loading from offset calibration block [24]. From simulation results, the calibration block increase comparator power consumption less than 8%. The input NMOS pair of the comparators is sized to have the comparator offset below the calibration range. The noise of the comparator is controlled by properly sizing the NMOS strobe switch at the bottom of the comparator [25].

III. Background Timing Skew Estimation

A conceptual ADC operation is shown in Fig. 8 to explain the proposed background timing skew estimation. The input signal and sampling clocks of the flash ADC (ϕ) and the SAR ADC (ϕ_X) are shown on the left. Reference voltages of the flash ADC which are equivalent to the MSB DAC level of the SAR ADC are shown in the middle. The LSB DAC level of the SAR ADC is shown on the right.

In the top of Fig. 8, the input signal is sampled by the flash ADC (ϕ) and the SAR ADC (ϕ_X) simultaneously. Thus, assuming the flash ADC is accurate, they sample the same input signal and coarse estimation from the flash ADC is accurate. In this example, the flash ADC output is 12. Although the flash ADC confines the SAR searching range between 32 and 96, due to the redundancy, the SAR search covers a wider range than necessary. The SAR conversion output (D_{LSAR}) nominally falls between 32 and 96. However, when ϕ and ϕ_X are not aligned as shown in the bottom of Fig. 8, the flash ADC and the SAR ADC sample different values of the input signal and the coarse estimation from the flash ADC will be inaccurate. However, due to the redundancy, the SAR finds the accurate final value. In this case, the SAR conversion output (D_{LSAR}), 18 in this example, goes beyond the nominal range.

The effect of the timing skew can be summarized from the histogram of D_{LSAR}. Fig. 9 shows an example of the D_{LSAR} histogram with and without the timing skew error. In this ideal case, D_{LSAR} is confined in the nominal range and the density is uniform. However, with a timing skew, some of the D_{LSAR} codes at the edge spills over to cover the inaccurate estimation from the flash ADC and this increases the variance of the D_{LSAR}

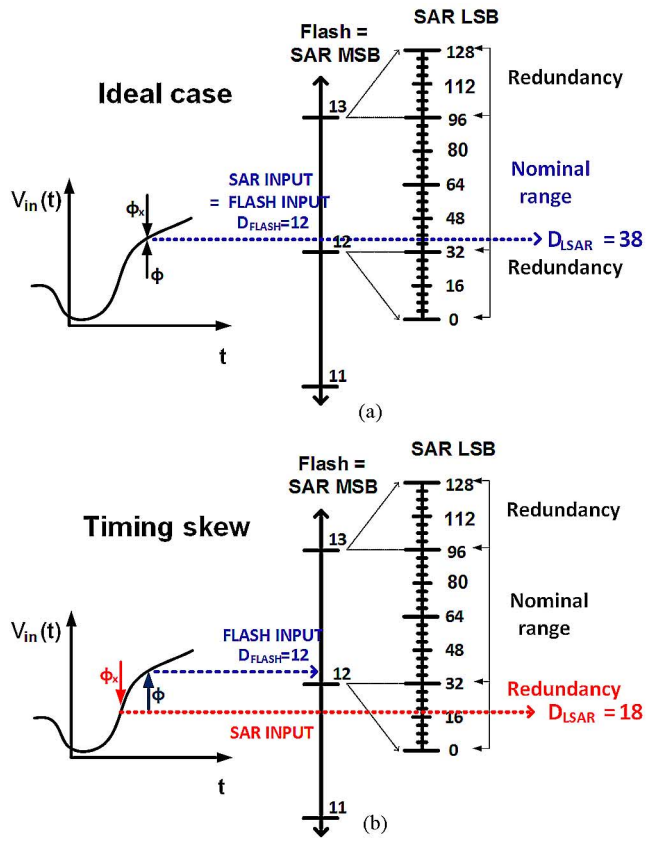


Fig. 8. Conceptual diagram of the ADC operation. Top: ideal case without timing skew. Bottom: realistic case with timing skew.

histogram. Thus, timing skew can be estimated from the variance of D_{LSAR}. To verify the idea, behavioral simulations are performed and plotted in Fig. 10. In this simulation, two single input signals with different frequencies and two tone signals are applied. 128 K (2^{17}) data values are used to calculate each variance value on the plot. As expected, $\mathrm{VAR}(D_{LSAR})$ is minimized when the timing skew is zero, regardless of the input frequency and the number of tones.

The proposed variation based timing skew estimation can also be explained mathematically as follows. Assuming the

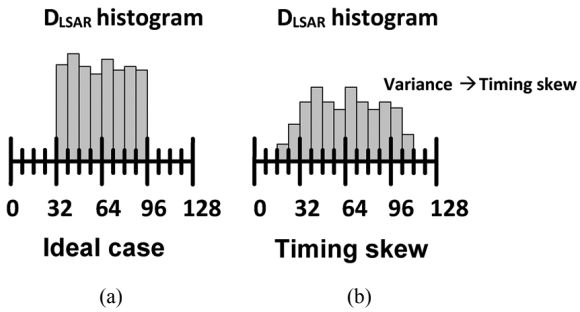


Fig. 9. Examples of the $\mathrm{D_{LSAR}}$ histogram (a) without timing skew and (b) with timing skew.

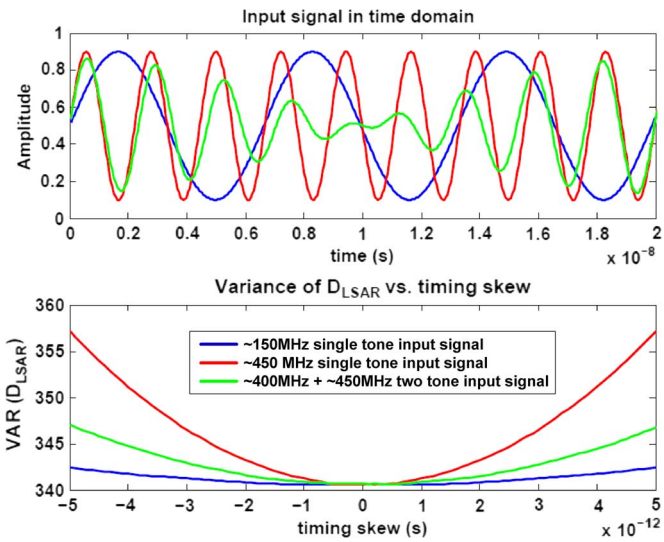


Fig. 10. Behavioral simulation result: Timing skew vs. $\mathrm{VAR(D_{LSAR})}$.

error due to the timing skew is small and covered by the redundancy in the SAR ADC, the channel output, $\mathrm{D_{CHANNEL}}$, is completely determined by the sampled value of the SAR ADC. Then, the digital output of the flash ADC and the digital output of each channel can be written as

$$\mathrm{D_{FLASH},}_i[\mathrm{n}] = v_{\mathrm{IN}}(\mathrm{nT}) + \mathrm{Q_{FLASH},}_i[\mathrm{n}] \quad (1)$$

$$\mathrm{D_{CHANNEL},}_i[\mathrm{n}] = v_{\mathrm{IN}}(\mathrm{nT} + \Delta \mathrm{t}_i) + \mathrm{Q_{CHANNEL},}_i[\mathrm{n}] \quad (2)$$

where $\mathrm{D_{FLASH},}_i[\mathrm{n}]$ and $\mathrm{Q_{FLASH},}_i[\mathrm{n}]$ are the digital output of the flash ADC resolved for the ith channel and the quantization noise of $\mathrm{D_{FLASH},}_i[\mathrm{n}]$ respectively, $\mathrm{D_{CHANNEL},}_i[\mathrm{n}]$ and $\mathrm{Q_{CHANNEL},}_i[\mathrm{n}]$ the digital output and the quantization noise of ith channel respectively, and $\Delta \mathrm{t}_i$ the timing skew between the flash ADC and ith SAR ADC channel. From these equations, the variance of the $\mathrm{D_{LSAR},}_i$ can be expressed as

$$\mathrm{VAR}\left[\mathrm{D_{LSAR},}_i[\mathrm{n}]\right] = \mathrm{VAR}\left[\mathrm{D_{CHANNEL},}_i[\mathrm{n}] - \mathrm{D_{FLASH},}_i[\mathrm{n}]\right] \quad (3)$$

$$= \mathrm{E}\left[\left(v_{\mathrm{IN}}(\mathrm{nT} + \Delta \mathrm{t}_i) - v_{\mathrm{IN}}(\mathrm{nT})\right)^2\right] + \mathrm{Q^2_{CHANNEL},}_{i,\mathrm{rms}} + \mathrm{Q^2_{FLASH},}_{i,\mathrm{rms}} \quad (4)$$

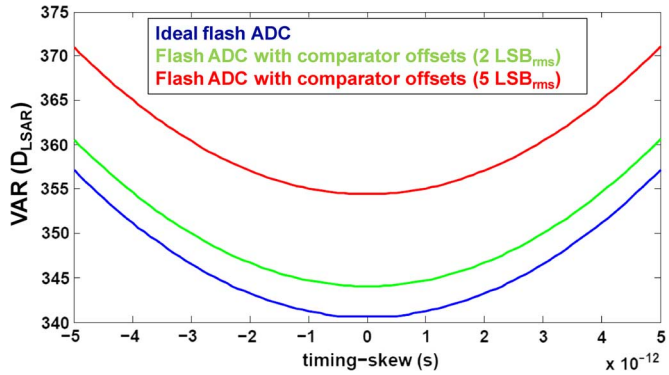


Fig. 11. Behavioral simulation result with comparator offsets in the flash ADC.

where $\mathrm{Q^2_{CHANNEL},}_{i,\mathrm{rms}}$ and $\mathrm{Q^2_{FLASH},}_{i,\mathrm{rms}}$ are the quantization noise power of the ith channel ADC and the quantization noise power of the flash ADC output for the ith channel respectively. Equation (4) shows that $\mathrm{VAR}[\mathrm{D_{LSAR},}_i[\mathrm{n}]]$ is a function of $\Delta \mathrm{t}_i$ and it is minimized when $\Delta \mathrm{t}_i$ is zero. Equation (4) also indicates that minimizing $\mathrm{VAR}[\mathrm{D_{LSAR},}_i[\mathrm{n}]]$ is equivalent to finding a least-mean-square (LMS) error approximation between the two sampled signals: $v_{\mathrm{IN}}(\mathrm{nT})$ and $v_{\mathrm{IN}}(\mathrm{nT} + \Delta \mathrm{t}_i)$.

It is important to point out that the propose calibration does not detect timing skew $(\Delta \mathrm{t}_i)$ directly, but measures the power of the error cause by timing skew $(\mathrm{E}[(v_{\mathrm{IN}}(\mathrm{nT} + \Delta \mathrm{t}_i) - v_{\mathrm{IN}}(\mathrm{nT}))^2])$. Thus, for the same accuracy of variance measurement, the accuracy of timing skew can be different for different input signal. For a band-limited input signal, the error from a given timing skew is proportional to the derivative of input signal. Thus, the calibration result with lower derivative may have larger residual timing skew but the same power of skew tones.

In the previous explanation, an ideal flash ADC is assumed. However, it is important to consider nonidealities of the flash ADC, such as offset and noise of the flash comparators. First, the comparator offsets in the flash ADC have a negligible impact to the timing skew estimation. It is true that the comparator offsets in the flash ADC provide inaccurate coarse estimation to the SAR ADCs and increase the range of $\mathrm{D_{LSAR}}$. However, since the polarity and amplitude of the comparator offsets do not change, they can be distinguished from timing skew errors easily. The behavioral simulation result, plotted in Fig. 11, shows that the comparator offsets in the flash ADC shift the $\mathrm{VAR(D_{LSAR})}$ curve upward, but do not change the fact that $\mathrm{VAR(D_{LSAR})}$ is minimized when the timing skew is zero. In this simulation, comparator offsets with two different rms values are tested with a ~450 MHz, -2 $\mathrm{dB_{FS}}$ input signal.

The noise of the comparators in the flash ADC has different impacts on the $\mathrm{D_{LSAR}}$ histogram. Because the polarity and the amplitude of the comparator noise vary randomly, it is difficult to distinguish the error caused by the comparator noise in the flash ADC from the error caused by timing skew with one sample. However, if the histogram and variance of the $\mathrm{D_{LSAR}}$ are calculated from a sufficiently large number of samples, the effect of the comparator noise can be controlled statistically and distinguished from the effect of timing skew. In other words,

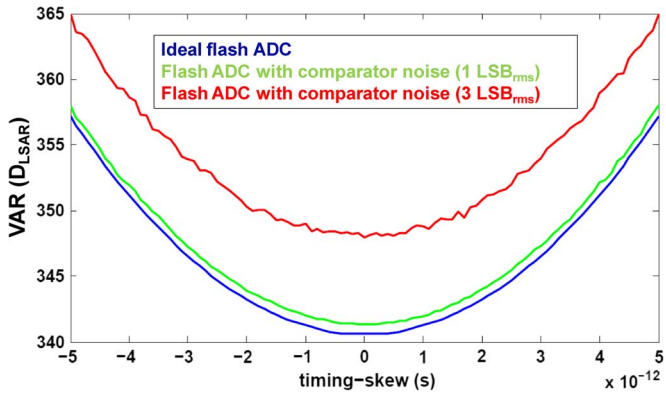


Fig. 12. Behavioral simulation result with comparator noise in the flash ADC.

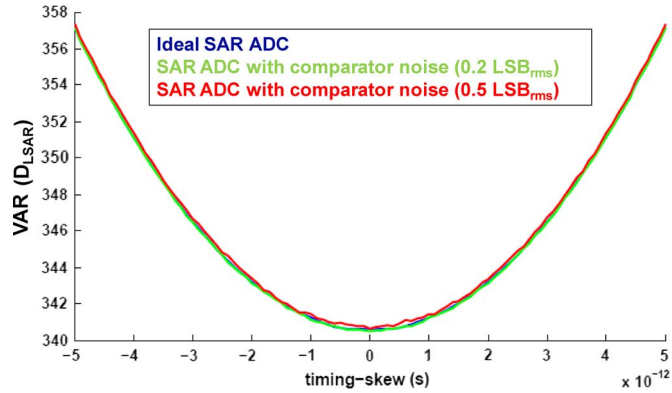


Fig. 13. Behavioral simulation result with comparator noise in SAR ADC.

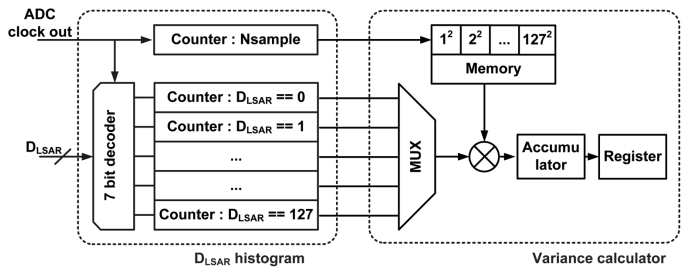


Fig. 14. Block level implementation of timing skew calibration.

although the variance of D_{LSAR} is increased due to the comparator noise, the amount of increase is nearly the same for every $VAR(D_{LSAR})$ calculation with sufficient samples. It is because the noise power of the comparators is constant. To demonstrate this, the effects of the comparator noise are simulated with behavioral models. The comparator noise with two different RMS values is tested with a ~450 MHz, -2 dB_{FS} input signal. As before, 128 K (2^{17}) samples are used to calculate each variance value on the plot. Fig. 12 shows that the noise of the comparators in the flash ADC adds noisy patterns, which degrades the sensitivity of the timing skew calibration. However, by using more samples for the variance calculation, the impact of the flash comparator noise can be reduced. The maximum comparator noise that can be controlled statistically is limited by the redundancy range between the flash and SAR conversion (±32 LSB in this prototype). Because the noise of comparator is stored in the redundancy range of D_{LSAR}, comparator noise larger than the redundancy range is clipped and distorted in D_{LSAR}. In this case, the effect of comparator noise cannot be controlled statistically.

The noise of the comparators in the SAR ADCs also affects the histogram of D_{LSAR} and sensitivity of the calibration. Since the noise power of the SAR comparator is typically significantly lower than that of the flash ADC comparators and usually kept well below 1 LSB, it typically has a negligible impact. The behavioral simulation result shown in Fig. 13 confirms it. Although only the effects of the flash and SAR comparator noise are explained above, other noise sources, such as reference voltage noise and thermal noise of sampling capacitors have the same effect on the variance.

Fig. 14 shows an example of block level implementation of the timing skew calibration. Assuming random input signal, variance can be simplified as $VAR(D_{LSAR}) = E[D_{LSAR}^2] = 1/Nsample \times \Sigma\{k^2 \times histogram(D_{LASR} == k)\}$ over all k. For this prototype case, 128 counters are required to generate histogram of D_{LSAR}. These counters operate at the speed of single channel clock, 125 MHz for this prototype. Another counter is needed to count the total number of samples. Once the total number of samples reaches to a certain value, counters for D_{LSAR} histogram hold their values and the variance is calculated. Because k^2 calculation is repetitive for each variance calculation, it can be replaced by a memory or lookup table. Note that, during the most of the calibration time, only counters are active to generate histogram which can be implemented with low power consumption.

The proposed timing skew calibration has a few limitations. First, the input signal must be busy or active and have sufficient amplitude coverage, so that the input signal crosses at least one of the reference voltages of the flash ADC. This is because the proposed methods detect the difference of the sampled input signal between the two independent ADCs. Second, the input frequency should not be an integer multiple of fc, where fc is the conversion rate of each channel. Although this is a pathological case, if the input frequency is an integer multiple of fc, each channel samples the same signal repetitively which lead to zero variance of D_{LSAR}. Finally, because the proposed methods rely on statistics of the input signal, input characteristic should be maintained during the timing skew calibration. For example, if the input signal is busy, but appears more frequently where D_{LSAR} is close to the edges of nominal range, 32 and 96 in the prototype for example, $VAR(D_{LSAR})$ can increase without timing skew. A detection circuit that qualifies the input waveform based on the flash ADC and SAR outputs can be used to perform calibration only when the input signal meets the qualification for the activity and amplitude coverage.

IV. Experimental Results

A prototype ADC is fabricated in 65 m CMOS process. To minimize the effects of package parasitics, the chip is bonded to the test board directly. The LVDS output signals of the ADC are captured by a logic analyzer directly without decimation.

Fig. 15 shows the measured spectrum with a low-frequency (11 MHz) input signal. The spectrum of a single channel result is shown on the left and the spectrum of the time-interleaved result

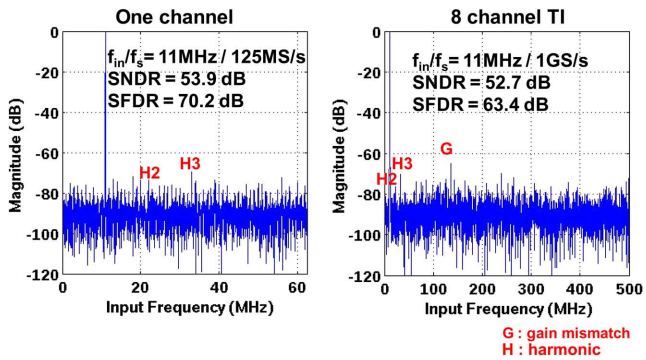


Fig. 15. Measured spectrum before calibration: single channel result (left) and time-interleaved result (right) with a low frequency input signal at 11 MHz.

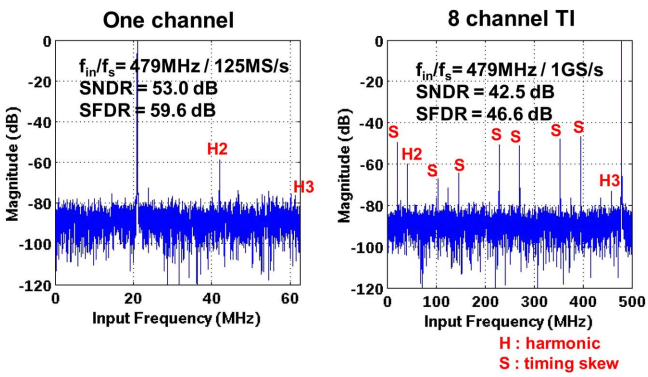


Fig. 16. Measured spectrum before calibration: single channel result (left) and time-interleaved result (right) with a Nyquist rate input signal at 479 MHz.

is plotted on the right. A typical single channel achieves 53.9 dB SNDR and 70.2 dB SFDR. The SNDR in the time-interleaved result shows 52.7 dB SNDR and 63.4 B SFDR. Considering that the input frequency is very low, the errors from the timing skew are negligible. The 1.2 dB SNDR degradation in the TI result is due to the gain and offset mismatches between the channels. For single channel result at low frequency input, the effect of offset, timing skew, gain mismatch, and clock jitter are not dominant error sources. From the fact that SNDR is not limited by lower harmonics but noise, crosstalk through shared reference voltage between channels is believed as a liming factor of single channel SNDR.

Fig. 16 shows the measured spectrum with an input signal close to the Nyquist rate (479 MHz). A typical single-channel result shows only a slight degradation in SNDR compared with the low-frequency test. This means that clock jitter does not limit the performance. Although the SNDR of a single channel is maintained above 53 dB, the time-interleaved spectrum suffers from large tones caused by timing skews between channels. As a result, SNDR and SFDR are limited to 42.5 dB and 46.6 dB respectively without calibration. Estimated timing skew from the skew tone power is about 2.7 ps rms.

Next, the timing skew calibration method described in Section III is performed. Fig. 17 shows the $\mathrm{VAR}(\mathrm{D_{LSAR}})$ against the coarse delay control codes of the SAR sampling clocks. Here, 128 K data values are used to calculate each

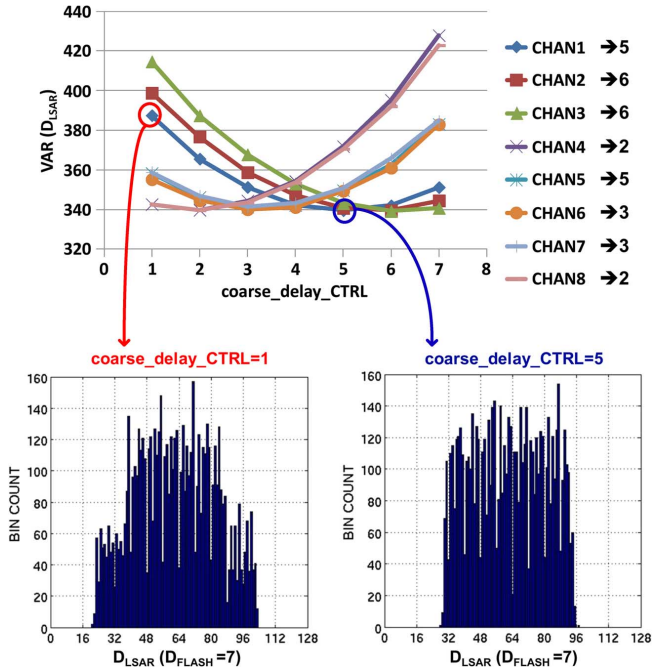
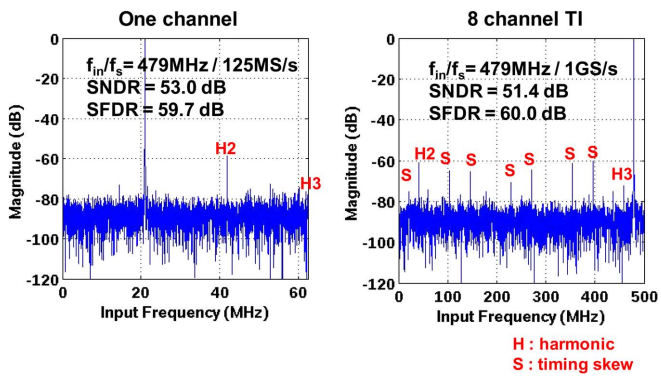


Fig. 17. Measured variance of $\mathrm{D_{LSAR}}$ against coarse delay control code of SAR ADC sampling clock (top) with the examples of the $\mathrm{D_{LSAR}}$ histogram for channel 1 (bottom).



(a) (b)

Fig. 18. Measured spectrum after background timing skew calibration: (a) single-channel result and (b) time-interleaved result with a Nyquist rate input signal at 479 MHz.

variance. All channels show a smooth curve with one minimum. Each channel chooses the coarse delay control code which corresponds to minimum $\mathrm{VAR}(\mathrm{D_{LSAR}})$. The same process is repeated for the fine delay control code to complete the calibration. To demonstrate the possibility of background calibration and to avoid possible errors from a deterministic input signal, the calibration is performed over four different input frequencies and two different input amplitudes, and the differences are found to be insignificant.

Fig. 18 shows the measured spectrum after timing skew calibration. A typical single channel result is the same as before calibration. However, the error tones in the time-interleaved result are significantly reduced by the calibration. SNDR and SFDR are improved to 51.4 and 60.0 dB, respectively. Estimated clock jitter from SNR degradation at Nyquist rate input

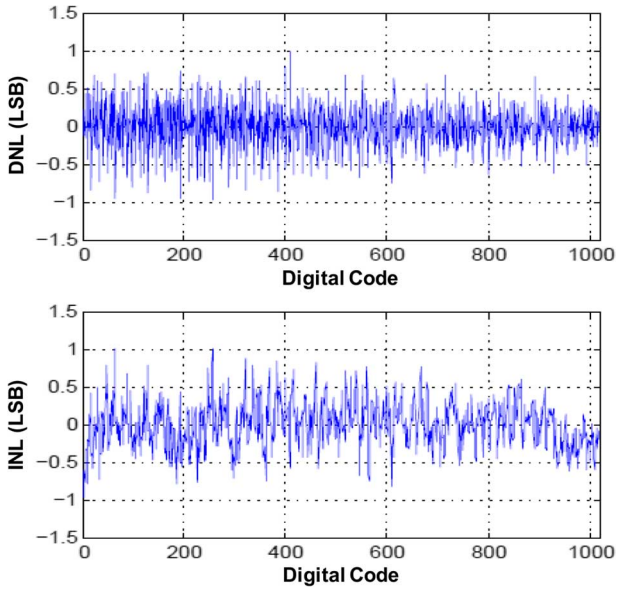


Fig. 19. Measured INL/DNL of the ADC.

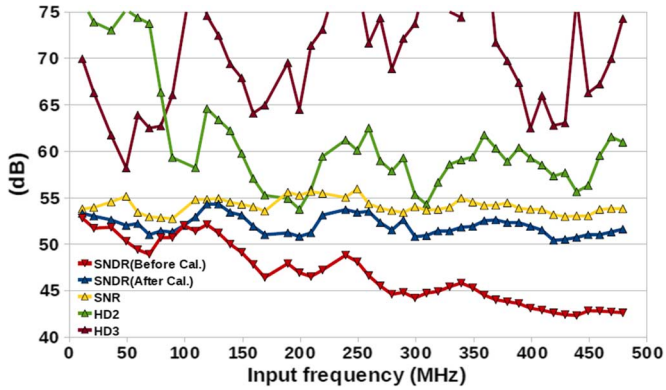


Fig. 20. Measured SNDR/SNR/HD2/HD3 versus input frequency of TI channels.

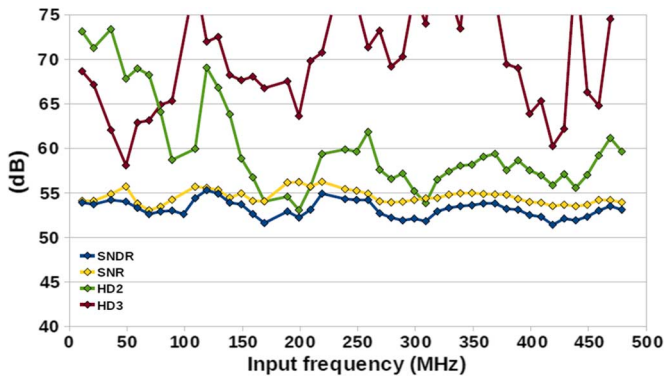


Fig. 21. Measured SNDR/SNR/HD2/HD3 versus input frequency of a single channel.

frequency compared to SNR with very low frequency input is about 0.3 ps rms. Timing skew is estimated from the residual skew tone power after calibration which is about 0.55 ps rms, which is slightly worse than the calibration resolution of 0.4 ps, believed to be due to the relatively low sensitivity and structured noise in variance versus skew characteristic.

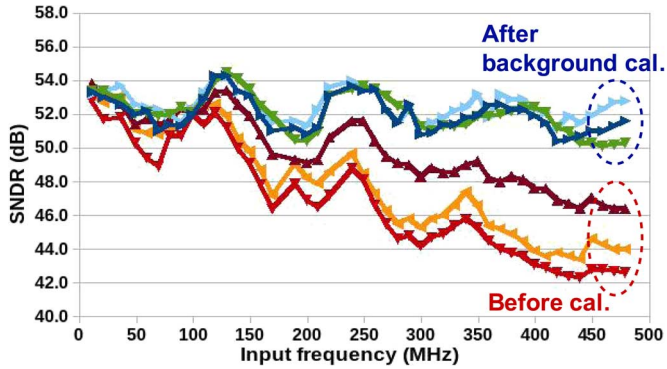


Fig. 22. Measured SNDR versus input frequency from three different chips.

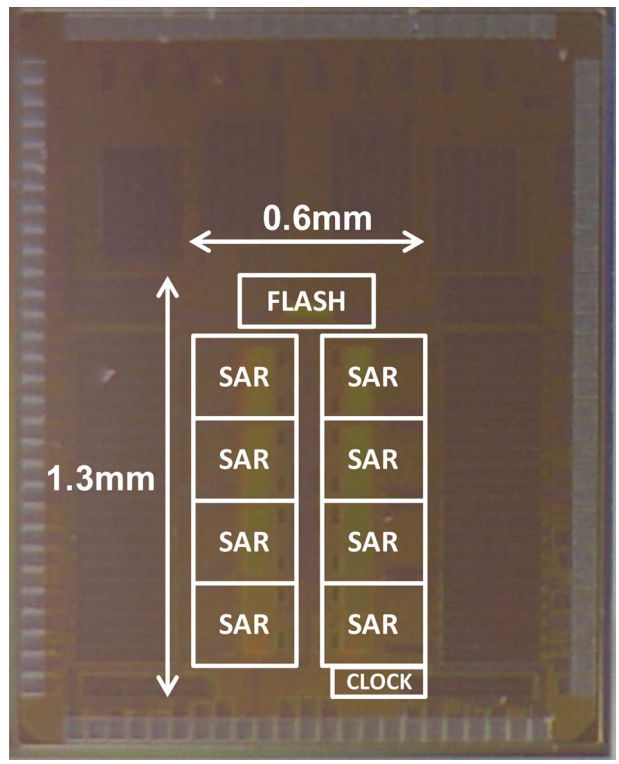


Fig. 23. Die photograph of the time-interleaved SAR ADC.

The power consumption of this prototype is 18.9 mW (clock 3.34 mW, flash ADC 5.04 mW, SAR ADCs 9.18 mW, reference 1.35 mW), which corresponds to 62.3 fJ/step FoM. 1 V reference voltage is provided from an external source. The power consumption of the digital circuits for background timing skew estimation is not included. Because timing skew does not change frequently, the calibration is not required to run continuously all the time. It may be initiated only when the chip is powered on and when temperature or voltage fluctuation is detected. Then, the power consumption of the calibration circuit is insignificant and can be ignored. The INL/DNL plots are shown in Fig. 19.

To highlight the effectiveness of the timing skew calibration, SNDR/SNR/HD2/HD3 versus input frequency is plotted in Fig. 20 (TI channels) and in Fig. 21 (one channel). It clearly shows that SNDR drop at high input frequency is recovered by background calibration. It is also notable that SNDR plot has a

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	This work	ISSCC 2013 Hong	VLSI 2013 Chiang	VLSI 2012 Stepanovic	VLSI 2012 Sahoo	ISSCC 2011 Mulder
Architecture	TI SAR	TI SAR	PIPE	TI SAR	PIPE	TI PIPE
Technology	65nm	45nm	65nm	65nm	65nm	40nm
Supply Voltage (V)	1.0	1.2	1.0	1.2	1.2	1.0/2.5
Sampling rate (GS/s)	1.0	0.9	0.8	2.8	1.0	0.8
Resolution (bit)	10	9	10	11	10	12
SNDR @ Nyquist (dB)	51.4	51.2	52.2	48.2	52.4	59.0
Power (mW)	18.9	10.8	19.0	44.6	32.9	105
FoM (fJ/step)	62.3	40.5	71.4	75.8	96.6	180.2

repetitive pattern over input frequency in both before and after calibration, which exists in single channel result as well. This suggests that it is a problem of single channel, not a problem caused by TI structure. The SNDR waviness is believed to be caused mainly by data-dependent disturbances on the external input network. Neither the SAR nor the flash sampling capacitors are cleared of previous charge before sampling. Thus, the charge corresponding to the previous sample of each channel disturbs the input network. The disturbance is minimum when the input frequency coincides with the channel sampling rate. In this case, each channel sees the same input voltage in consecutive samples, thus the sampling capacitors already have correct charge before sampling, minimizing the disturbance on the input network. Conversely, when the input frequency is at the Nyquist rate of each channel, the consecutive samples of each channel undergoes the maximum change, thus introducing the largest disturbance on the input network. One possible solution to mitigate this data-dependent input network disturbances is adding a reset phase to clear the charge in the previous sample. This reset phase does not eliminate disturbance on the input network, but makes disturbance constant and data-independent. The variation of HD2/HD3 between the channels is believed to be caused by data-dependent power supply noise whose manifestation is different between channels due to different power supply routing and physical locations on the die.

The measurement results of three different chips are plotted in Fig. 22. Before calibration, the SNDR is spread widely and limited by the timing skew for all three chips at high input frequencies. After calibration, the three chips provide similar performance with 1.2 dB SNDR variation at the Nyquist input rate.

The die photograph of the prototype ADC is shown in Fig. 23. The active area of the ADCs is highlighted and occupies 0.78 mm^2. The unused area of the chip is filled with decoupling capacitors.

Table I summarizes the performance with a comparison to previously published work with $f_S > 0.8$ GS/s, SNDR > 45 dB, and FoM < 180 fJ/step [26]. This work compares favorably with published work.

V. CONCLUSION

This paper describes a time-interleaved SAR ADC with background timing skew calibration. A full-speed flash ADC shared among eight SAR ADC channels provides MSBs to SAR ADCs in one cycle which enhances the conversion speed and saves power consumption of the SAR ADCs. The flash ADC is also used as a reference of timing skew calibration which allows background calibration. A prototype ADC is fabricated in 65 nm CMOS process and achieved 51.4 dB SNDR at 1 GS/s with 18.9 mW, which is comparable to the state-of-the-art. The corresponding FoM of 62.3 fJ/step is the best result among GHz, 10 bit range ADCs in similar technology.

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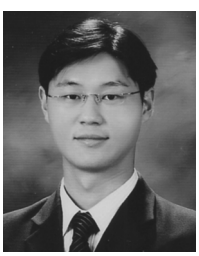

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